University of West Bohemia

Faculty of Electrical Engineering

Department of Applied Electronics and Telecommunications

A Role of Sigma Delta Modulators in Touchscreen Controllers

Report on the Doctoral Thesis

Author:
Ing. Lukas Palocko

Supervisor:
prof. Ing. Jiri Pinker, CSc,

June, 2019

University of West Bohemia

Declaration

I hereby submit this work for state doctoral exam. I declare that all work has been done independently. All used literature and sources are cited and listed in this document. Only legal and licensed software was used.

The doctoral thesis was worked out in Ph.D. study at the Department of Applied Electronics and Telecommunications, Faculty of Electrical Engineering, University of West Bohemia.

Candidate:
Ing. Lukas Palocko
Faculty of Electrical Engineering, University of West Bohemia
Department of Applied Electronics and Telecommunications
Univerzitní 26, Pilsen, 306 14, Czech Republic

Supervisor:
prof. Ing. Jiri Pinker, CSc,
Faculty of Electrical Engineering, University of West Bohemia
Department of Applied Electronics and Telecommunications
Univerzitní 26, Pilsen, 306 14, Czech Republic

Opponents:

.....

.....

.....

The report on doctoral thesis was delivered on: .....
The report on doctoral thesis was sent on .....

Defense of the doctoral thesis will take place on ..... before the committee for the study field Electronics at FEE UWB, Univerzitní 26, Pilsen, in the conference room ..... at .....

.....
Chairman of the department committee

Abstract

This doctoral work is focused on an analysis, modeling and prototyping of sigma-delta modulators. First, to identify properties of an application, particular attention is paid to the review of the Projected Capacitive Touch Technology (p-cap) sensors and the sensing strategies. Then, the target application - touchscreen systems - is introduced with a discussion of low-power Analog-to-Digital Converters (ADCs). The research of the power-efficient and the area-efficient analog to digital conversion identifies an ADC candidate. The ADC candidate, Sigma-Delta ($\Sigma\Delta$) converter, is introduced as well as the summary of a modulator diversity.

At the system and circuit level, this dissertation addresses low-power modulator design systematically from two aspects: external efforts considering target application and internal efforts considering modulator architectures and a circuit implementation. For internal efforts, thesis deals with synthesis and design considerations of modulators and gives a comparative study of the parameters variations such as OSR, OBG and the zero position. This part of the thesis also presents values of the coefficients, which are directly related to the circuit elements, as the consequence of the Dynamic-Range Scaling of the modulator. The demand for higher resolution of ADC results in the stability problem for high-order modulators. Thesis provides short review related to the maximum stable amplitude and opens a new discussion of the guantizer gain issues.

A primary aim of the doctoral thesis is to give a comprehensive overview of the methodology and design strategies to identify optimized circuit solution for low-power consumption and small silicon area. Then an estimation of circuit metrics has been identified as one of the most important task of the design strategy. The proposed methodology allows designer to consider an implementation of the circuit-level hierarchy with the system-level properties of the modulator. The outcome is a circuit optimization based on the gm/Id methodology for particular modulator topology. The optimum inversion level for individual MOS transistor is always an option of the trade-off between the power consumption and the silicon area.

Abstract

Táto dizertačná práca je zameraná na analýzu a modelovanie sigma-delta modulátorov. V primeranom rozsahu k práci, je predstavená Cieľová aplikácia zameraná na systémy dotykových obrazoviek. Ďalšou časťou úvodnej kapitoly je diskusia o možnostiach analógovo-číslicového prevodu so zameraním na nízku spotrebu. Zvláštna pozornosť je taktiež venovaná zhodnoteniu senzorov s kapacitným snímaním, ktoré sú využívané v moderných mobilných aplikáciách. V práci je tiež popísaný prieskum možnosti analógovo-číslicového prevodu s minimálnou spotrebou a plochou čipu, ktorý bol založený na datovej sade profesora Murmana. To umožňuje identifikovať vhodný typ A/Č prevodníka. Tato úvaha je prezentovaná v kapitole 1.1.4.

Jedna z hlavných častí, syntéza a rozprava o návrhu modulátorov, poskytuje komparačnú štúdiu rôznorodých parametrov, ako napríklad OSR, OBG a pozícia nuly prenosovej funkcie šumu (NTF). Práca prezentuje výsledky syntetizovaných koeficientov modulátorov, ktoré sú priamo zviazané s obvodovými prvkami ako dôsledok dynamického škálovania.

Práca si kladie za cieľ poskytnúť ucelený prehľad metodológie a návrhových postupov k identifikácii optimálneho obvodového riešenia (pre sigma-delta modulátory realizované spínanými kapacitormi) so zameraním na nízku spo-trebu a minimálnu plochu čipu. Hlavná pozornosť je zameraná na odhad metrík obvodu, ktoré sú výsledom optimalizačnej procedúry. Výhodou tejto metódy je kombinácia obvodovej hierarchie spolu s vlastnosťami na systémovej úrovni, ktoré vieme vyjadriť rovnicami. Výsledkom je optimalizácia obvodu založená na metóde gm/ids (transkonduktančná efektivita) ako dôsledok špecifikácie transkonduktančného aktívneho prvku, ktorá bola získaná na obvodovej úrovni. Optimálny stupeň inverzie pre samostatný MOS tranzistor je výsledkom kompromisu a rovnováhy medzi energetickou spotrebou, veľkosťou kremíkovej plochy a špecifikáciou obvodu.

Ďalšie hľadisko, ktorým je potreba sa zaoberať na základe požiadavky na vyššie rozlíšenie systému, je otázka stability modulátorov vyššieho stupňa. Ako dôsledok tejto problematiky je uvedené krátke zhrnutie poznatkov týkajúcich sa amplitúdy, pri ktorej je systém ešte stabilný. A zároveň práca otvára novú diskusiu venovanú kvantizačnému zisku.

Práca popisuje komplexnú stratégiu pri navrhovaní modulátorov, kedy je nutné brať v úvahu jednotlivé príspevky (s rôznou prenosovou funkciou) šumových zdrojov, ktoré prispievajú k celkového šumu mudulátora na výstupe a tým ovplyvňujú jeho dynamicky rozsah.

Contents

List of Acronyms **vii**

1 Introduction **1**
1.1 Motivation and Background 1
1.1.1 P-cap Sensor 1
1.1.2 System for Touch Detection 2
1.1.3 Analog Frond-end 3
1.1.4 Issues of Analog to Digital Converters 5
1.2 Problems and Questions 7
1.2.1 Research Objectives 9
1.2.2 Contributions of Doctoral Thesis 10

2 Sigma-Delta Modulators - State of the Art **13**
2.1 Basic of a Sigma-delta Conversion 13
2.2 Architectures of Sigma-delta Modulators 14

3 Synthesis and Design Considerations of Sigma-Delta Modulators **17**
3.1 Discrete-Time Sigma-Delta Modulator ($\Sigma\Delta$M) 17
3.2 Sizing of Capacitors 19
3.2.1 Voltage Supply and Coefficients Scaling 20
3.2.2 Transfer Function of Thermal Noise Sources 22
3.3 High-order $\Sigma\Delta$M Stability Issues 22
3.4 Analyzing Proposed Analog Frond-ends (AFEs) 23
3.5 Design Strategy of Optimization Procedures 25

4 Modeling and Validation of Sigma-Delta Converters **29**
4.1 Modeling of Sigma-Delta Converters 29

4.1.1 Configuration of Test Benches 30
4.1.2 Frequency Spectrum of Modulators 31
4.2 Validation of ΣΔM Sub-blocks 32

5 Transistor-level implementation of the ΣΔM 33
5.1 Operational Amplifiers 34
5.2 Regenerative Latch-based Comparators 37
5.2.1 One-stage Dynamic Comparators 38
5.2.2 Two-stage Dynamic Comparators 40

6 Conclusions 41
6.1 Summary 41
6.2 Future Work 43

List of Acronyms

$S\&H$	Sample-and-Hold
ΣΔ	Sigma-Delta
ΣΔC	Sigma-Delta Converter
ΣΔADC	Sigma-Delta ADC
ΣΔM	Sigma-Delta Modulator
μC	Microcontroller
AAF	Anti-aliasing filter
ADC	Analog-to-Digital Converter
AFE	Analog Frond-end
C2V	Capacitance to Voltage
CIFB	Cascade of Integrators in a Feedback Configuration
CIFF	Cascade of Integrators in a Feed-forward Configuration
CRFB	Cascade of Resonators in a Feedback Configuration
CRFF	Cascade of Resonators in a Feed-forward Configuration
CT-ΣΔM	Continuous-Time Sigma-Delta Modulator
DAC	Digital to Analog Converter
DFT	Dicrete Fourier Tranform
DR	Dynamic Range
DT-ΣΔM	Discrete-Time Sigma-Delta Modulator
ENOB	Efective Number of Bits

FFT	Fast Fourier Transform
FOM	Figure of Merit
GBW	Gain-Bandwith product
IBN	In Band Noise
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTF	Noise-transfer Function
OBG	Out-Band Gain
op-amp	Operational Amplifier
OSR	Oversampling ratio
OTA	Operational Transconductance Amplifier
p-cap	Projected Capacitive Touch Technology
PS	Power Spectrum
PSD	Power Spectral Density
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range
SNDR	Signal-to-Noise and Distorsion Ratio
SNR	Signal-to-Noise Ratio
SoC	system on a chip
SQNR	Signal-to-Quantization-Noise Ratio
STF	Signal-Transfer Function

List of Tables

3.1 The summary of modulators across different Out-Band Gain (OBG) when an input amplitude is 0.5V. 19

5.1 Ota metrics for the Simple one-stage Operational Transconductance Amplifier (OTA), 5.2 (a), Folded Cascode OTA 5.3 (b), and Two-stage OTA with the miller compensation. The estimation has been provided by the python script, that uses real data of the MOSFETs (1.2 device, technology node is $\approx 65\,nm$). The parameter of devices are follows: $(gm/Ids)_{Mx} = 15$, $L_n = L_p = 400\,nm$, VDD = 1.2V. 37

5.2 Ota metrics for the Simple one-stage OTA, 5.2 (a), Folded Cascode OTA 5.3 (b), and Two-stage OTA with the miller compensation. The estimation has been provided by the python script, that uses real data of the MOSFETs (1.8 device, technology node is $\approx 180\,nm$). The parameter of devices are follows: $(gm/Ids)_{Mx} = 15$, $L_n = L_p = 400\,nm$, VDD = 1.8V. . 38

Acknowledgments

I would like to express my first and foremost gratitude to Professor Jiri Pinker, my supervisor, for his patient guidance, enthusiastic encouragements and useful reviews of this research work. I would also like to thank Dr. Vjaceslav Georgiev, Head of the Department of Applied Electronics and Telecommunications of the University of West Bohemia for the many helpful discussions. He is the person who nudged me in the direction of analog integrated circuit design.

Furthermore, my deep thanks go to the members of AMS design team, STmicroelectronics s.r.o. in Prague, and especially to Pavel Krejci for his valuable comments and suggestions at the beginning of this research.

Next, I would like to extend my deep thanks to the senior members of the analog group of Adesto Technologies situated in Prague, for their teaching and guidance but also their useful critiques related to analog design.

I would also like to acknowledge my colleagues and friends, especially Jan Broulim, Pavel Broulim, Vaclav Divis, Ondrej Krpal and Jan Moldaschl for the many discussions, help and great encouragement.

A special thank goes to my family and my friends.

Finally and most especially, I am deeply grateful to my wife, Zuzka. Words alone cannot express what I owe her for her encouragements and patient love, both of which enabled me to complete this thesis. Life is filled with ups and downs, and her unfailing confidence in me allowed me to go through the whole process of writing my PhD thesis.

1 | Introduction

The current trend in system on a chip (SoC) design results in increasing requirements for individual building blocks, including ADCs. Modern ADCs require high resolution, high integration, low-power consumption, compatibility with digital CMOS processes and signal processing and still, low-cost competition. This thesis deals with a research on problems which must be addressed when facing a real touchscreen application.

1.1 Motivation and Background

Touchscreen interactive devices have become increasingly important in both commercial and consumer applications including mobile phones, tablets, laptops etc. There are several different touchscreen technologies, including analog resistive, projected-capacitive, surface capacitive, surface acoustic wave, infrared, camera-based optical, LCD in-cell, and force sensing, which were proposed during recent years [Wal12]. Today, the consumer electronics market, including phones, laptops, and tablets, is based on the p-cap.

In the last 5years, a p-cap has become a new standard of touchscreen. The main characteristics of touchscreen based on the p-cap are:

- Multiple simultaneous touches
- Extremely light touches with flick/swipe gestures
- Excellent optical properties

1.1.1 P-cap Sensor

There are two basic concepts of p-cap, *self capacitance* and *mutual capacitance*, where the difference between them is basically in how the electrodes are treated:

- **Self-capacitance** is based on a measurement of the distributed parasitic capacitance of an electrode to ground. The capacitance of an electrode is increasing when a finger is near the electrode. This situation is shown in Figure 1.1. The measured element is a charge stored in the distributed capacitance of an electrode. The result of the sensing based on a self-capacitance is two vectors of charge, $q_{\vec{xself}}$ and $q_{\vec{yself}}$:

$$q_{xself} = \begin{bmatrix} C_{self,x0}\Delta U & C_{self,x1}\Delta U & \dots & C_{self,xk}\Delta U \end{bmatrix}$$

$$q_{yself} = \begin{bmatrix} C_{self,y0}\Delta U & C_{self,y1}\Delta U & \dots & C_{self,yk}\Delta U \end{bmatrix}$$

  The main disadvantage of the self-capacitance is multi-touch detection, which is illustrated in Figure 1.3. Two and more touches can not be calculated using the mode based on the self-capacitance sensing.

- **Mutual-capacitance** is based on evaluation of the capacitance between a pair of electrodes. The value of the capacitance is decreased when a finger is near the pair of electrodes. In other words, the capacitance of a human body (to the ground) 'steals' some of the charge between the two electrodes, Figure 1.2.

  The mutual mode uses one geometrical pattern for driving the electrodes, and other pattern of the electrodes is used for sensing the mutual capacitances between the particular driving electrode and the sensing electrodes. The result of this evaluation is a matrix $(j \times k)$ of charge values:

$$q_{mutual} = \begin{bmatrix} C_{m11}\Delta U & C_{m12}\Delta U & \dots & C_{m1k}\Delta U \\ C_{m21}\Delta U & C_{m22}\Delta U & \dots & C_{m2k}\Delta U \\ \vdots & \vdots & \ddots & \vdots \\ C_{mj1}\Delta U & C_{mj2}\Delta U & \dots & C_{mjk}\Delta U \end{bmatrix} \tag{1.1}$$

  The main disadvantage is the evaluation time which is increasing with the number of force electrodes.

1.1.2 System for Touch Detection

As shown in Figure 1.4, the concept of a projected-capacitive touchscreen is composed of a sensor AFE, ADC, a circuit for digital signal processing, and Microcontroller (μC). One of the backbone block is the ADC which transforms analog information to the digital representation of a "touch" position.

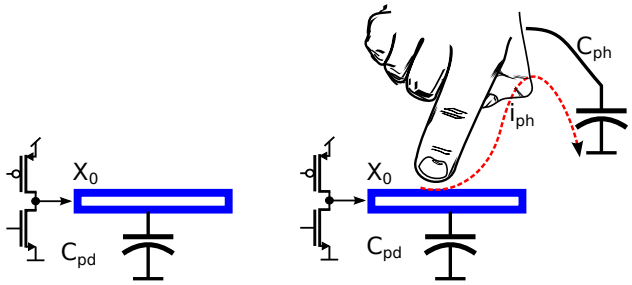

Figure 1.1: The concept of self capacitance: the capacitance of a single electrode to ground, C_{pd}, - no touch (left), the capacitance is increased by a human body capacitance, C_{ph}, to the ground - touch (right).

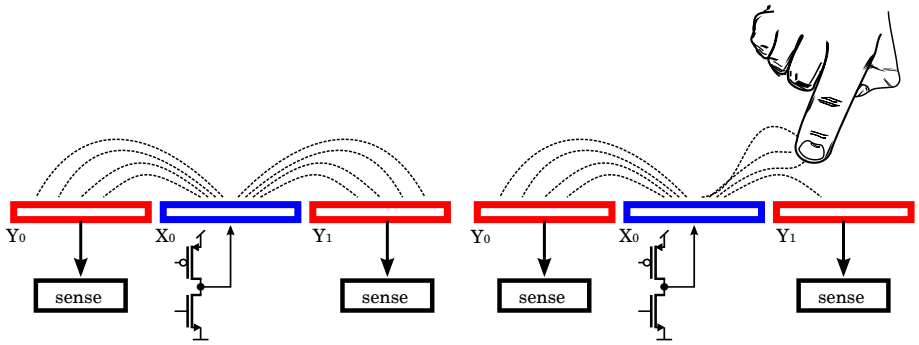

Figure 1.2: The concept of mutual capacitance: the capacitance between the pair of electrodes, X_0,Y_1, without touch (left), the capacitance is decreased, C_{X_0,Y_1}, when a finger is near to the pair of electrodes (right).

The resolution requirement of the ADC depends on several aspects, e.g., the voltage-level used for a scanning mechanism, input noise, and the performance of the AFE. Typically, A/D conversion of target application requires medium-to-high resolution, ranging from 8-bit to 12-bit. A medium-resolution conversion can not be sufficient if there is no charge compensation[1]. The combination of requirements including resolution, speed, and small die size, makes the design very challenging.

1.1.3 Analog Frond-end

Figure 1.5 shows possible implementation of an Analog-Front End AFE and the following stage, an analog to digital conversion. In this concept, FORCE

[1]Even if there is no touch, the capacitance of electrodes is not equal. This mismatch of capacitances influences the resolution.

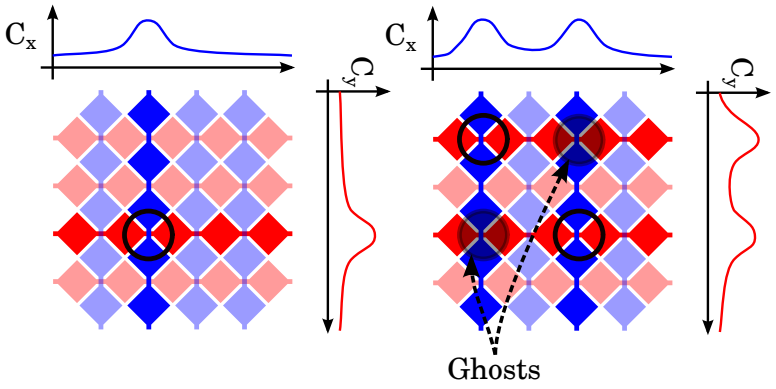

Figure 1.3: The idea of touch detection based on the self-capacitance: single (left) and multi touch (right).

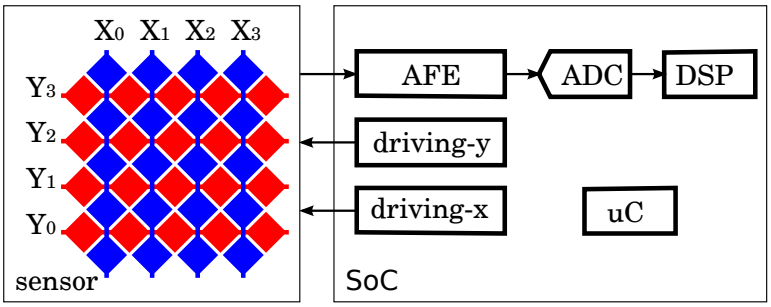

Figure 1.4: The example of a touchscreen system is composed of a p-cap sensor and a SoC.

and SENSE nodes are driving by TX block (with particular the voltage up to 12 V) and the output of the Capacitance to Voltage (C2V) block corresponds to the charge stored in capacitances C_M, C_F, C_S. We can write:

$$C_{Mtot} = C_{MP} + \Delta C_{MP} \tag{1.2}$$

$$C_{SPtot} = C_{SP} + \Delta C_{SP} \tag{1.3}$$

$$C_{FPtot} = C_{FP} + \Delta C_{FP} \tag{1.4}$$

The first term of Equations 1.2, 1.3 and 1.4 corresponds to the parasitic capacitance and the second one, delta of these capacitances, ΔC_{MP}, ΔC_{FP}, ΔC_{SP} is the product of the touch on a panel. Generally, there are two problems:

- ΔC_{MP}, ΔC_{FP}, ΔC_{SP} are small fraction of parasitic capacitances, C_{MP}, C_{FP}, C_{SP}.
- C_{MP}, C_{FP}, C_{SP} have not the same value across the matrix array and also they are changed from panel to panel.

This drawbacks are (typically) solved by the charge compensation technique and the accumulation of the voltage at the C2V output. The voltage is then translated (by the ADC) to the digital form, where a digital post-processing is used.

To save current consumption we can:

- exclude the charge compensation technique. As a result, timing and the control system of the AFE can be significantly reduced. Also there is a demand for the higher resolution of the ADC. Trade-off must be considered.
- remove the power-hungry charge pump. This significantly reduces Signal-to-Noise Ratio (SNR) of the charge to voltage conversion and deep analysis of this issue must be performed.

The topics, questions and answers related to the points above are beyond the scope of the this work, but the basic introduction to discussed issue is given in Section 3.4.

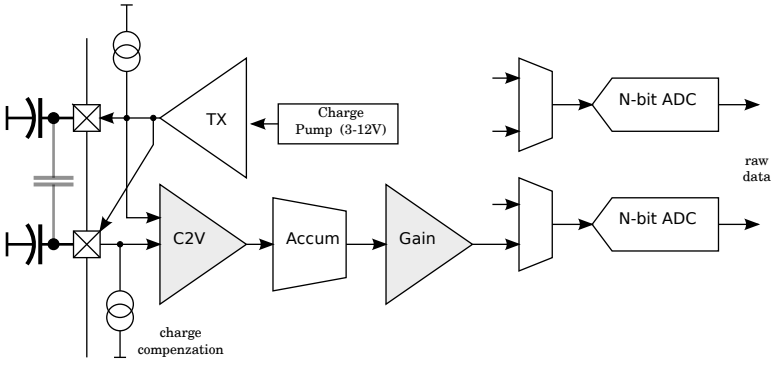

Figure 1.5: The possible implementation of the AFE displays.

1.1.4 Issues of Analog to Digital Converters

The ADC can be implemented by a large diversity of architectures. The choice of an architecture depends on the resolution, speed, the size of an

active area, power requirements of a specific application. The comparison of ADC architectures with different speed, resolution, die size, and power consumption is not a trivial task. There are several comparative researches of energy-efficient ADCs presented in [Jon11b] and [Jon13]. Another comparative study should be focused on area efficiency of ADC architectures. An empirical design optimization approach of area efficiency is given by Jonsson, where [Jon10] is focused on the impact of scaling device technology on ADC performance, and [Jon11a] discusses area efficiency of different ADC architectures.

Author is presenting four surveys of state-of-the-art ADC Integrated Circuits (ICs) published in the recent years (2013-2015) based on Murmann dataset [Mur]:

- *First survey* is shown in Figure 1.6 (top), where the energy per Nyquist sample is plotted over the Signal-to-Noise and Distorsion Ratio (SNDR) for different families of ADCs. The Figure points out that the most power-efficient solutions for low-speed, medium-to-high resolution application are based on the Successive Approximation Register (SAR) ADC and $\Sigma\Delta$ ADC.

- *Second survey* is shown in Figure 1.6 (bottom), where the frequency, $f_{inhl} = f_{snyq}/2$, is plotted over the SNDR for different families of ADCs.

- *Third survey* is shown in Figure 1.7 (top), where the area per effective quantization-step, $A_q = Area/2^{EONB}$, is plotted over the SNDR for different families of ADCs.

- *Fourth survey* is shown in Figure 1.7 (bottom), where the area per effective quantization-step, A_q, is plotted over the frequency, f_{inhl}, for different families of ADCs

Due to the advantages including ultra-low power consumption, simple architecture, and suitability for multi-channel conversion, the SAR ADC has been widely used in touchscreen applications. However, when the application requires high-resolution, such an architecture of ADC offers several drawbacks including large switching power, die size, and high sensitivity to parasitic capacitance.

The alternative architecture based on the $\Sigma\Delta$ modulation is able to achieve high-resolution with relaxed matching requirements. This is also

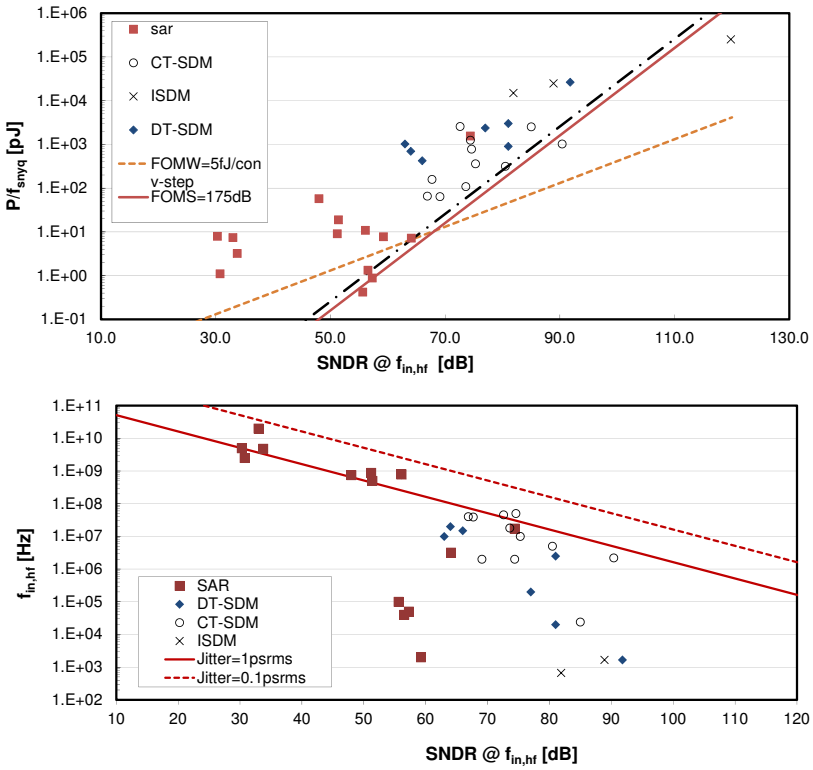

Figure 1.6: The comparison of published ADCs in recent years (2013-2015) based on the Murmann dataset [Mur].

shown in Figure in 1.6, where the state-of-the-art of low-power A/D conversion is given by SAR ADCs for medium-to-high resolution. For the resolution $\geq$ 12 bits, the state-of-the-art is appointed by Sigma-Delta Converters ($\Sigma\Delta$Cs). To distinguish limits of architectures based on $\Sigma\Delta$ conversion, the legend of the chart labels (denotes) different modulators used for $\Sigma\Delta$ conversion. In next chapters and section, author will be focused only on surveys and a research of $\Sigma\Delta$Ms.

1.2 Problems and Questions

Many articles, dissertations and books, which are dedicated to sigma-delta conversion, deal with one or two of the three type knowledges. The first consists in discovering new system-level solution, wheras the second proposes

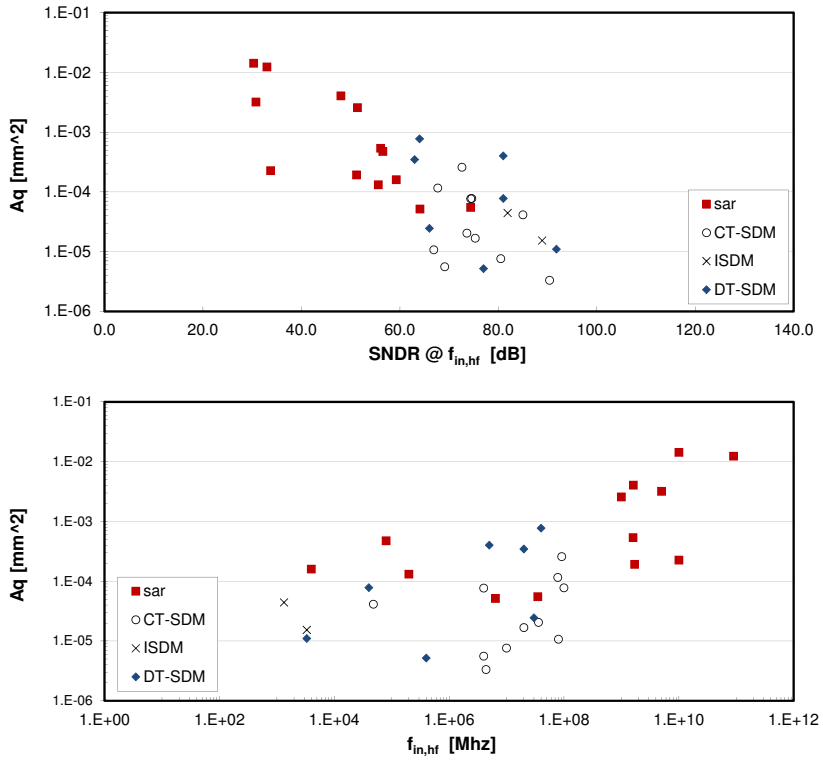

Figure 1.7: Published ADCs in recent years (2013-2015) based on the Murmann dataset [Mur].

new circuit implementation. The last one is a general analysis of modulators where the non-ideal circuit components are discussed. The wide scope of the research carried out on sigma-delta modulation makes the design steps and decisions more and more complicated. Circuit designers face problems of decisions related to the right architecture. On the other hand, system architects do not take into account circuit and technology limits. Design procedure is always an iterative process, but significant personal and financial resources can be saved when the limits of the technology, circuit implementations or system-level architecture are identified as soon as possible.

Therefore, the main contribution of this work is not the discovery of new circuits, but lies in providing a general vision of the modulator diversity and a progress track as well as some hints on where to look in the immense forest of circuit implementations.

1.2.1 Research Objectives

The main objective of the work, which includes this doctoral thesis as one part of the complex tasks related to design system on chip, is to investigate power-efficient solution of analog to digital conversion at both system and circuit level with focus on ΣΔCs. Generally, the dissertation will addresses the following aspects:

- Analyzing and identifying the impact of ΣΔM architectures on its performance and power consumption. The objective is to offer a reference for selecting power-efficient ΣΔM schemes given by different application scenarios.
- Exploring and proposing power-efficient ΣΔM architectures and the associated design strategies. Demonstrating their advantage through a comparative study of various ΣΔMs. The objective is to provide the highest performance, power-aware solutions with the smallest silicon die size required in touchscreen applications, specially, in sensing of a capacitive touchscreen.
- Investigating and proposing power-efficient circuit solutions to be embedded in the particular ΣΔM architecture. The objective is to explore methodology and design strategies, which lead to establish a feasibility study of the circuit implementation. These results determine technology process, personal and financial resources, timing of the project.

To accomplish these aspects several objectives of the dissertation must be specified:

- Basic exploration of the p-cap sensors and sensing strategies which address modern devices like phones, tablets, laptops and also control panels.
- Analysis of possible AFE architecture, which is focused on limits and requirements of the following stages.
- Exploration of the power-efficient and area-efficient analog to digital conversion to identify limits of the particular type of ADC.
- Synthesis of modulators (in different architecture configurations: CIFB, CRFB, CIFF, CRFF) including the comparative study of the parameter variation such as OSR, OBG and zero position.

- Evaluation the impact on the circuit elements as a consequence of (i) various topologies of the modulator and (ii) values of the input/output swing, which is a function of power supply.
- Discussion of the stability issue for high-order modulators and an analysis of the maximum stable amplitude for particular configuration.
- Evaluation of the particular noise contribution to the total input referred noise of the modulator.
- Estimation of metrics at circuit-level such as open-loop gain, noise, GBW, settling and slewing time, etc.
- Implementation of Dynamic-Range Scaling of the modulator, which address target input/output swing of the blocks.
- Optimization of the circuit-level implementation that is based on the synthesis and analysis at system-level.
- Optimization of the transistor-level implementation that is base on the gm/Id methodology (find optimum inversion level for particulate MOS transistor).
- Exploration and development methodology of design procedures, which enables the designer to identify parameters (circuit metrics) at different abstraction levels.

1.2.2 Contributions of Doctoral Thesis

This subsection presents contributions of doctoral thesis, which are divided to several types of contributions:

1. Confirmation and expansion of an existing model (i.e. evaluating the effects of a change in condition; providing an experimental assessment of a specific aspect of a model):

- Evaluation of the particular noise contribution to the total input referred noise of the modulator. Due to properties of $\Sigma\Delta$M (noise shaping converter), the transfer function of the noise source to output of the modulator must by considered and computed. The original solution is presented by the [SSST05] that discusses Cascade of Integrators in a Feed-forward Configuration (CIFF) topology. This methodology has been extended to Cascade of Integrators in a Feedback Configuration

(CIFB) topology and has been implemented by Python scripts, which determines total integrated thermal noise.

2. Combining two or more ideas and showing that the arrangement reveals something new and useful:

- One of the most important perspective - the estimation of circuit metrics - has been developed and this procedure is described in Section 3.5. The proposed methodology shows steps and optimized procedures to achieve lower level of the current consumption or silicon area for the specific parameters of the target application. This methodology is based on ideas:

  - pre-computed lookup tables of a mosfet device [PGAJ17].
  - design strategy of $\Sigma\Delta$M given by [SP17].
  - state-space description of $\Sigma\Delta$Ms [SP17].

  The advantage of proposed method is the combination of the circuit-level hierarchy and the system-level description using system equations. The outcome is optimized circuit (or a part of circuit) as a consequence of the OTA metrics that are defined by the system-level hierarchy. The methodology is extended to transistor-level, where the optimization of circuit elements (mosfet devices) is based on the gm/Id methodology. The optimum inversion level for particular MOS transistor is an option of the trade-off between the power consumption, silicon area and circuit specification.

3. Demonstrating a concept – proving that something is feasible and useful; or that something is infeasible and explaining why it fails:

- One of the main parts - synthesis and design considerations of modulators - describes the comparative study, which including variations of the parameters such as OSR, OBG and zero position. The thesis discusses also the coefficients, which are directly related to circuit elements, for different architecture configurations such as CIFB, CRFB, CIFF, CRFF. Implementation of Dynamic-Range Scaling of the modulator, which addresses target input/output swing of the blocks, has been developed (realized by Python scripts).

- Study of the circuit elements as a consequence of (i) various topologies of the modulator, (ii) the input/output swing (which is strong related

to a value of the power supply) and (iii) topology of active block, has been accomplished.

4. Implementing a theoretical principle – showing how it can be applied in practice; making ideas tangible; how something works in practice; and what its limitations are

- The demand for higher resolution of ADC can be met by the addition of more integrators into series or by increasing the number of quantization levels. Then the discussion of the stability problem for high-order modulators and an analysis of the maximum stable amplitude for particular configuration is needed. There is a lot of research work related, but mostly done on the theoretical level and inconvenient for practical purposes. Thesis offers a detailed description of the quantizer gain behavior (in term of the stability issue), which is the product of the high non-linear component. This illustrates practical explanations and also results, which identify limits of the topology. The discussion of the maximum stable amplitude are also presented in this thesis (Section 3.3).

5. Providing a new solution to a known problem and demonstrating the solution's efficacy:

- The analysis of possible AFE architecture that excludes the charge compensation technique is presented. Only the basic estimation has been accomplished, but this scope of the work needs a special attention. The feasibility study has to identify problems and provide answers and solutions. This issues are described in Section 3.4.

- Research of the power-efficient and area-efficient analog to digital conversion based on the Murmann dataset [Mur] point the ADC candidate type. The alternative architecture (to SAR ADC) based on the $\Sigma\Delta$ modulation is able to achieve high-resolution with relaxed matching requirements. The origin of this thesis is arisen from a question: "Is the $\Sigma\Delta$ converter the better solution of an analog to digital conversion for touchscreen controller?". The motivation of the doctoral thesis as a consequence of this question is covered in Subsection 1.1.4.

2 | Sigma-Delta Modulators - State of the Art

The sigma-delta modulators arise from oversampling converters which were invented as the technology-driven solutions to the overall task of signal acquisition including antialiasing, sampling and quantization.

The benefits of ΣΔ conversion can be summarized as:

- High-order Anti-aliasing filter (AAF) is not necessary.
- Thanks to combination of an oversampling and decimation operation, a part of the quantization noise can be eliminated.
- The digital filter and decimator are easily implemented by the standard cells. This is a major advantage due to the technology scaling.
- High resolution can be achieved even when a 1-bit quantization is performed.

ΣΔCs provide more resolution enhancement as described above. This extra resolution enhancement is given by a technique called "noise shaping".

The implementation of these principles in real hardware, especially when considering ICs, entails careful interplay between signal theory and implementation technology. These two parts cannot be separated.

2.1 Basic of a Sigma-delta Conversion

Figure 2.1 shows the basic concept of the ΣΔ converters, which includes the AAF and the Sample-and-Hold ($S\&H$) circuit at the input. The input circuit is followed by the ΣΔM and digital part of the circuit, the decimator.

The circuit is composed by the following blocks:

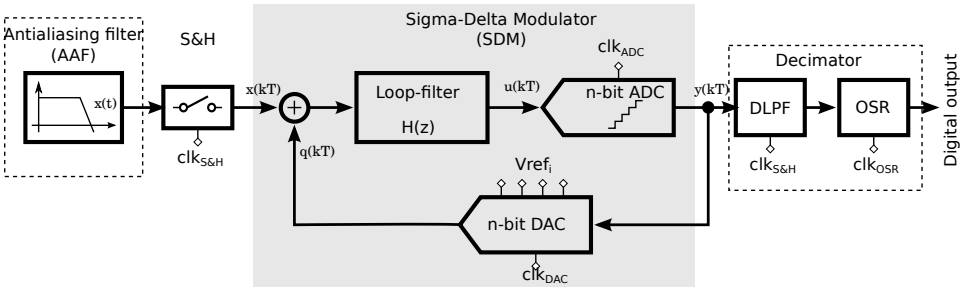

Figure 2.1: Concept of the sigma-delta converters.

- **AAF** is a low pass analog filter, used to avoid aliasing during the sampling operation. A high-order AAF is not needed, because the sampling frequency, fs, is far away from the maximum frequency of band-limited input signal.

- ΣΔM is a feedback system, where the oversampling and quantization noise-shaping is used to reduce the In Band Noise (IBN) and to increase the Dynamic Range (DR) of the AD conversion. The quantization noise, which is produced by low-resolution quantizers (typically 1-5 bits) is shaped by the loop filter with the $H(z)$ characteristic.

- **Decimation filter** is a high-selectivity digital filter used to remove the shaped quantization noise at the output of the ΣΔM. The output rate is defined by the oversampling frequency, f_s. The reduction to the Nyquist frequency, f_{NQ}, is performed by the decimator.

2.2 Architectures of Sigma-delta Modulators

Benefits of the conversion based on ΣΔ modulator (the oversampling and noise shaping) result in increasing interest in this field. Several types of ΣΔMs were discover during past decades.

There are several ways how to reduce the quantization noise power, $N_{\sigma^2_{\hat{e}_Q}}(f)$, and increase the DR of the modulator. The first way of tuning the modulator performance is setting on the number of quantization levels. The second and third way are tied to modulator order and Oversampling ratio (OSR), respectively.

The performance of the ΣΔMs is generally obtained by the characteristic properties of main functional block and OSR. Figure 2.2 shows the multidimensional flow of ΣΔM architectures.

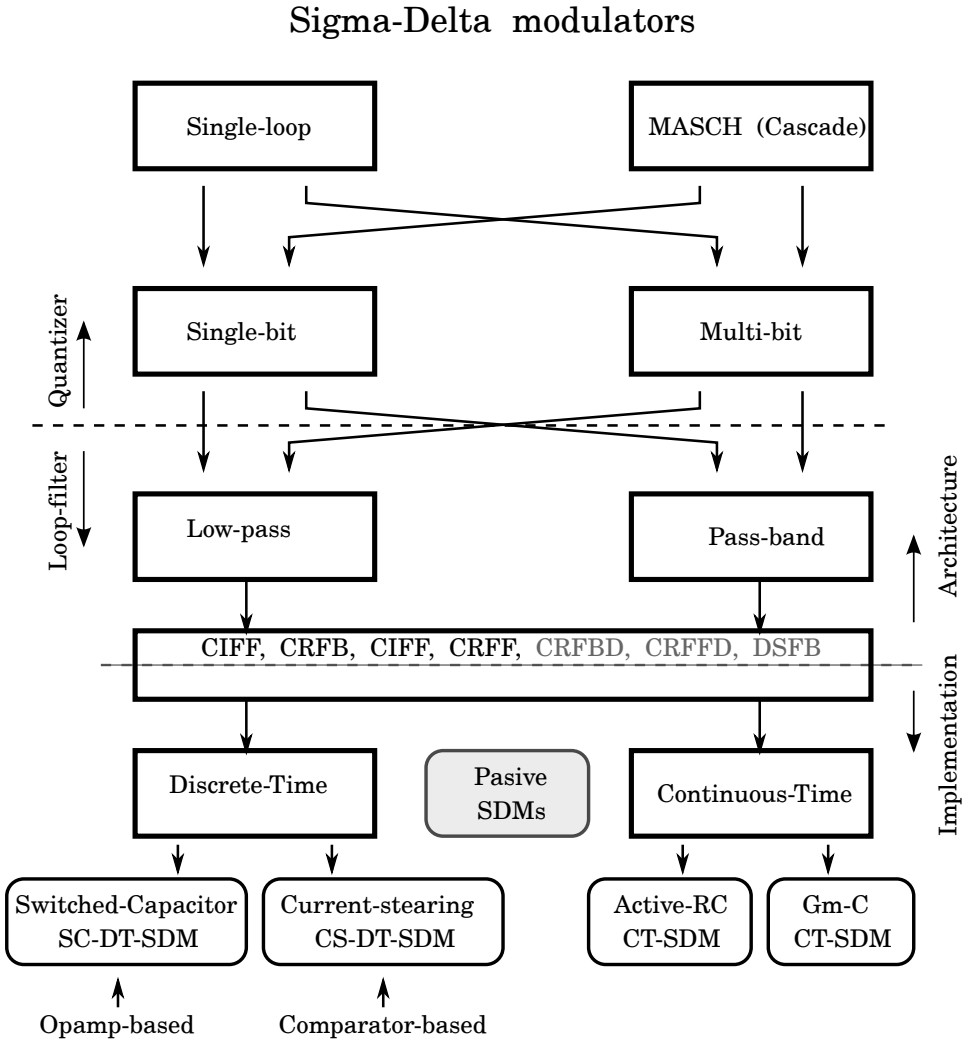

Figure 2.2: The summarization of the ΣΔM architectures.

There are two ways of modulator improvements provided by the quantization. The number of quantizers distinguish two main topologies:

- **Single-loop** ΣΔM.
- **Cascade** ΣΔM.

The resolution of embedded quantizers defines next two categories:

- **Single-bit** ΣΔM.

- **Multi-bit** ΣΔM.

Another building block is the loop-filter, which also has significant impact on the noise-shaping. There are other two ways modifying the modulator. The first demand on the characteristic of the loop-filter (low-pass, band-pass):

- **Low-Pass** ΣΔM.
- **Band-Pass** ΣΔM.

The second way of characteristic modifications is achieved by the implementation of a loop-filter. Two main types of modulators can be classified as:

- **Discrete-Time Sigma-Delta Modulator (DT-ΣΔM)**.
- **Continuous-Time Sigma-Delta Modulator (CT-ΣΔM)**.

Extending the first-order ΣΔM from more then two to an arbitrary *Lth*-order loop-filter is referred as high-order single-loop ΣΔM. Different single-loop topologies exist to implement a Noise-transfer Function (NTF) . These topologies can divided into two classes: *multiple feedback (FB)* and *feedforward (FF)*. In term of a chain of integrators or resonators, four main types of topology result:

- **CIFB** is the chain of cascaded delayed integrators with distributed feedback.
- **CIFF** is the chain of cascaded delayed integrators with feedforward summation.
- **Cascade of Resonators in a Feedback Configuration (CRFB)** is the chain of resonators (non delayed integrators with local resonator feedback) with distributed feedback.
- **Cascade of Resonators in a Feed-forward Configuration (CRFF)** is the chain of resonators (non delayed integrators with local resonator feedback) with feedforward summation.

There are also combinations of these configuration.

3 | Synthesis and Design Considerations of Sigma-Delta Modulators

The complexity of various topology, architecture and optimization parameters of ΣΔM lead to a huge number of the possible implementation. This chapter covers the investigation of several topologies of ΣΔM, including CIFB, CIFF, CRFB, CRFF.

3.1 Discrete-Time ΣΔM

To find impact of topology, we let start by the describing of a linear model (the second-order modulator is assumed), which can be covered by NTF and Signal-Transfer Function (STF), where NTF for maximum OBG is:

$$NTF_{|OPT=0} = \frac{1.0}{z^2}\left(1.0z^2 - 2.0z + 1.0\right) \tag{3.1}$$

$$NTF_{|OPT=1} = \frac{1.0}{z^2}\left(1.0z^2 - 1.9998z + 1.0\right) \tag{3.2}$$

and STF = 1. When we require STF flat, coefficients of the modulator, b_1, b_2, must be set to zero. The linear model does not describe a non-linearity of the quantizer, which affects NTF by a non-constant quantizer gain. The quantification of non-linearity effects of the quantizer can be realized in time domain by differential equations, which can be transform to state-space form. Discrete-time state-space matrices correspond to the modulator that can be expressed as follows:

$$\dot{x} = \boldsymbol{A_D}\boldsymbol{x} + \boldsymbol{B_D}\begin{bmatrix} u \\ v \end{bmatrix} \tag{3.3}$$

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_1 & -k_1 \\ b_2 & -k_2 \end{bmatrix} \begin{bmatrix} u \\ v \end{bmatrix} \tag{3.4}$$

$$\boldsymbol{y} = \boldsymbol{C_D x} + \boldsymbol{D_D} \begin{bmatrix} u \\ v \end{bmatrix} \tag{3.5}$$

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_0 & 0 \end{bmatrix} \begin{bmatrix} u \\ v \end{bmatrix} \tag{3.6}$$

ABCD matrices of state-space form are shown in Equations 3.7 and 3.8 for modulators in CIFB and CIFF configuration.

$$ABCD_{CIFB} = \begin{bmatrix} 1.000 & -0.000 & 0.216 & -0.216 \\ 1.000 & 1.000 & 0.000 & -0.775 \\ 0.000 & 1.000 & 0.000 & 0.000 \end{bmatrix} \tag{3.7}$$

$$ABCD_{CIFF} = \begin{bmatrix} 1.000 & -0.000 & 1.000 & -1.000 \\ 1.000 & 1.000 & 0.000 & -2.000 \\ 0.000 & 1.000 & 0.000 & 0.000 \end{bmatrix} \tag{3.8}$$

This matrices describe modulator which is not in scaled form (there is no "signal limit" of particular node). For real modulator these matrices must by scaled to fit maximum input/output swings of embedded blocks. When each modulator is characterized by the same NTF an output bitstream must be the same for each architecture of the modulator and then an input of the quantizer must by the same across architecture. The difference between modulators lies in the feedback and feed-forward coefficients, which represent a ratio of the capacitors. Then the power consumption and the silicon area are not the same as the consequence of the variation of the coefficients.

The modulators have been synthetized by the demand of maximum OBG, which for the second order system is 4. The amount of OBG has important impact on the circuit stability. Second order modulator is conditional stable [Sch05] even for maximum value of OBG, but high value of OBG has influence on the Signal-to-Quantization-Noise Ratio (SQNR) and Spurious-free Dynamic Range (SFDR). Table 3.1 summarizes results from synthesis of the equation 3.1. We can also see that the gain of quantizer (in this example, two level of quantization is performed) changes significantly.

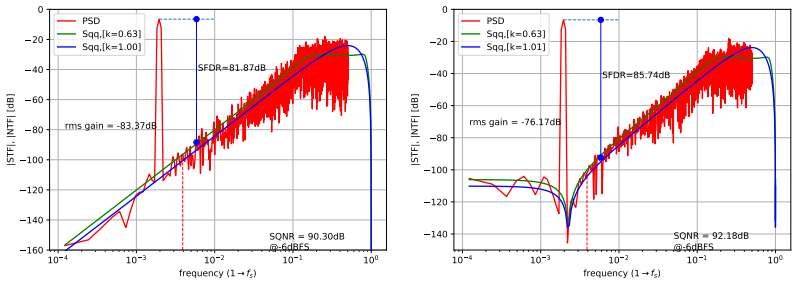

Figure 3.1: Spectrum of modeled ΣΔM in the CIFB configuration. Left: zero in DC, right: optimized position of zero.

Table 3.1: The summary of modulators across different OBG when an input amplitude is 0.5V.

	NTF	OBG	SFDR	SQNR	k_GAIN
0	$\frac{1.0z^2-2.0z+1.0}{1.0z^2-1.2174z+0.44}$	1.5	73.79	84.60	1.78
1	$\frac{1.0z^2-2.0z+1.0}{1.0z^2-0.9117z+0.29}$	1.8	75.87	88.92	1.26
2	$\frac{1.0z^2-2.0z+1.0}{1.0z^2-0.75157z+0.23}$	2.0	79.24	88.30	1.12
3	$\frac{1.0z^2-2.0z+1.0}{1.0z^2-0.2456z+0.06}$	3.0	84.36	84.31	0.76
4	$\frac{1.0z^2-2.0z+1.0}{1.0z^2+0.02z-0.01}$	4.0	82.23	84.52	0.63

Figure 3.1 shows a typical spectrum for the second order ΣΔM, which corresponds to fourth row of Table 3.1. We see that NTF (blue curve) does not fit the spectrum from the simulation of the state-space description. This discrepancy (shifting in horizontal axis) is influenced by the real quantizer gain.

3.2 Sizing of Capacitors

Sizing of capacitors is an important aspect in design consideration, which have an impact on the silicon area and power consumption. The relationship between coefficient and relative value of particular capacitor can be expressed:

$$a_1 = \frac{C_1 V_{ref}}{C_2} = \frac{C_1 V_{DD}}{C_2} \tag{3.9}$$

$$b_1 = \frac{C_1 V_{FS}}{C_2 M} \tag{3.10}$$

$$a_2 = \frac{C_{DAC2}}{C_{I2}} VDD \tag{3.11}$$

$$c_1 = \frac{C_{S2}}{C_{I2}} VDD \tag{3.12}$$

It should be noted that these equations are valid only in cases when $a_1 = b_1$. This enables to use the same capacitor for the sampling and the summation operation. To specify absolute value of capacitors, one more constrain is needed. This constrain is derived from noise specification. The maximum noise for full-scale input amplitude can be expressed as:

$$v_n^2 = \frac{\frac{(\frac{V_{dd}}{2})^2}{2}}{10^{\frac{SNR}{10}}} \tag{3.13}$$

Using well-know "kT/C" theory we can express relationship between C_1 and v_n^2 (for single-ended implementation)[Sch05]:

$$v_n^2 = \frac{kT}{C_1} \frac{BW}{\frac{f_s}{2}} = \frac{kT}{OSR\, C_1} \tag{3.14}$$

Using equation 3.13 and 3.14, the capacitor of the first integrator can be specified.

3.2.1 Voltage Supply and Coefficients Scaling

Up to this point voltage supply of ΣΔM has not been discussed. This subsection describes extension of this procedure and presents results of coefficients and circuit elements as a function of power supply.

The input/output swing of the modulator nodes, $\{x_1, x_2, ..., x_n\}$, are directly linked to the modulators coefficients. The next consideration is then focused on relation between coefficients (output of a synthesis) and input/output swing, which is defined by supply voltages. There is one more variable - saturation voltages of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors - that is need to take into consideration.

Thesis denotes this voltage margins as V_{SOFT} for VDD and VSS lines separately. At this point of a design flow, design architect can perform first analysis of Figure of Merit (FOM), which is related to silicon area and power consumption. This also creates the first specification of blocks, which lies at circuit-level hierarchy.

Lets consider an example of the ΣΔM with two variables, supply voltage, V_{DD}, and the voltage for which the transistors leave saturation, V_{SOFT}, as follows:

$$V_{DD} = \begin{bmatrix} 1 & 1.2 & 1.5 & 1.8 & 2.5 & 3.3 \end{bmatrix}$$

$$V_{SOFT} = \begin{bmatrix} 0.1 & 0.2 & 0.3 & 0.4 \end{bmatrix}$$

To get available voltage swing at internal nodes, normalized V_{SOFT}, must be defined. It can be realized by matrix of a scale factor, which is set in the our example as follows:

$$SF = \begin{bmatrix} 0.500 & 0.600 & 0.750 & 0.900 & 1.250 & 1.650 \\ 0.500 & 0.600 & 0.750 & 0.900 & 1.250 & 1.650 \\ 0.500 & 0.600 & 0.750 & 0.900 & 1.250 & 1.650 \\ 0.500 & 0.600 & 0.750 & 0.900 & 1.250 & 1.650 \end{bmatrix} \tag{3.15}$$

and the matrix of available normalized voltage swing at one of the internal nodes is then:

$$Vav^{x1}_{NORM} = \begin{bmatrix} 0.800 & 0.833 & 0.867 & 0.889 & 0.920 & 0.939 \\ 0.600 & 0.667 & 0.733 & 0.778 & 0.840 & 0.879 \\ 0.400 & 0.500 & 0.600 & 0.667 & 0.760 & 0.818 \\ 0.200 & 0.333 & 0.467 & 0.556 & 0.680 & 0.758 \end{bmatrix} \tag{3.16}$$

The columns of the matrix represent supply voltages and the rows stand for voltage margin, V_{SOFT}, which is related to saturation voltages. The first and last column represent a modulator with 1V 3.3V supply voltage respectively. The worst case of the voltage swing in the example is $Vav^{x1}_{NORM} = 200mV$. It is a realistic description of the case when folded cascode OTA is applied to the design with 1V supply voltage. The 200 mV of voltage headroom is allocated for every MOSFET device in the stack. On the other side, the counterpart corresponds to $Vav^{x1}_{NORM} = 0.939mV$. This is a little bit theoretical limit where the basic one-stage OTA or two-stage OTA is used for 3.3V supply voltage. The voltage margin of 100 mV per MOSFET is too low in practical design (to allow this situation, the MOSFET must be

biased into deep week inversion, which results in a huge device). And also there is no voltage margin related to process and temperature variations. This problems associated to MOSFET biasing are discussed in Chapter 5. To express absolute capacitance values across particular voltage swing (is the function of supply voltage and voltage margin, V_{SOFT}) coefficients of ΣΔM are need to be computed first. Coefficients are product of the synthesis with the input parameter $Vav^{xk}_{NORM\,i,j}$. When the coefficients are established (for particular VDD and V_{SOFT}), absolute values of capacitances are a function of total integrated thermal noise.

The next subsection is focused on thermal noise estimation, where every thermal noise source is identified and the particular contributions to total integrated output thermal noise is described.

3.2.2 Transfer Function of Thermal Noise Sources

A study to identify contribution of every thermal source is presented in this Subsection. First, it is necessary to express transfer function from the input of an every thermal source to the output of a modulator. In the case of CIFF topology, two noise sources are related to the each integrator, input referred voltage noise source v_{ni}, and output refereed voltage noise source v_{no}. Each noise source has different transfer function to the output and then, the contribution of particular noise source to the total output noise of the modulator is different. It should be noted that for varying topology of the ΣΔM, transfer function of the particular noise source is not the same. In another words, even for the same integrators, the total output thermal noise has different value for particular ΣΔ topology.

Generally, OSR decreasing with the demand for increasing bandwidth of the system where the blocks are at a speed limit defining by a technology node. Also one could decrease the Gain-Bandwith product (GBW) of OTAs to save power (and also area per block), but at the cost of increasing number of blocks (transconductance amplifiers or compactors). Up to this point it is impossible to say, which strategy is better for power/area optimization, but an optimum exist for a specific application.

3.3 High-order ΣΔM Stability Issues

Section 3.1 describes variations of the quantizer gain for different values of OBG and the amplitude of input sinusoidal signal. This variation of the quantizer gain has important impact on the stability of a third-order (and more) ΣΔMs.

The location of poles and zeros of the third-order discrete-time ΣΔM are shown on Figure 3.2 across different values of OBG. The left side of Figure shows poles and zeros for constant gain (k=1). The right side of the Figure shows poles and zeros of NTF for equivalent quantizer gain extract from the simulation. The last pair of poles (OBG =2) are outside of the circle (not visible in Figure) and then, system is unstable. This experiment was performed for an amplitude of the input sinusoidal signal, $A_{sin} = 0.5$.

The reason why this instability occurs can be explained using Figure 3.3. There are dashed and solid lines for particular input parameter OBG of the synthesis. The solid lines correspond to desired NTF, which have quantizer gain=1. Because the quantizer gain is not constant, NTF is influenced by this variability and the NTF is changed (dashed line). Generally, when the OBG is increasing, the equivalent gain is decreasing. For the last cases of the example presented in figure 3.3, magenta lines, OBG is set to 2, the equivalent gain drop to zero and system is unstable.

3.4 Analyzing Proposed AFEs

In Subsection 1.1.3, thesis describes charge to voltage conversion base on the charge compensation technique. In this Section we are focusing on the case when charge compensation technique is not present. Let us suppose the parameters of the sensor model (p-cap sensor):

- Self capacitance, C_{SP} C_{FP}, is varying from 20pF to 150pF.
- Delta of self capacitance corresponds to touch, ΔC_{SP} ΔC_{FP} , is approximately 10fF.
- Mutual capacitance, C_{MP}, is varying from 0.5pF to 3.5pF.
- Delta of mutual capacitance correspond to touch, ΔC_{MP}, is approximately 80fF - 100fF.

To get Efective Number of Bits (ENOB), signal to noise ratio must be computed. The basic estimation can be done by simple kT/C theory (noise of amplifier is neglected), but in this case the result is inaccurate. We stop here but this scope of the work needs a special study to investigate several aspects of AFE including:

- SNR of the sensor and C2V conversion. For this purpose, the model of the sensor must be created with no hidden states. Using special

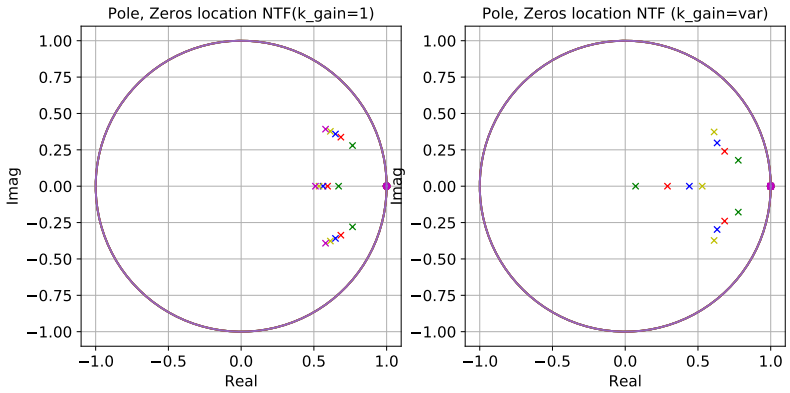

Figure 3.2: Poles-zeros location as a function of required OBG.

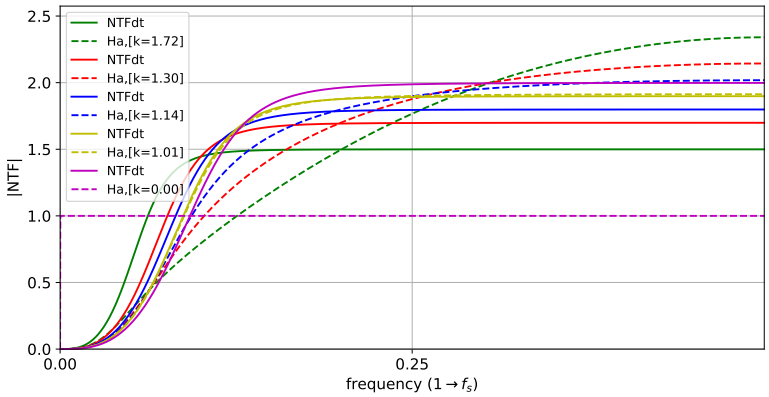

Figure 3.3: NTF is affected by the variety of quantizer gain.

noise analysis, Periodic Steady State Noise Analysis (PNOISE) with shooting algorithm, the total output sampled noise at the C2V output can be computed.

- effects of the parasitic capacitances (C_{SP}, C_{MP}) and their variation on the total output sampled noise must be quantified.
- maximum value of the static and dynamic error related to the C2V conversion.
- OTA candidate and its output swing,
- analysis of the oversampling technique to reduction the noise floor.

3.5 Design Strategy of Optimization Procedures

Considering all aspects that are mentioned in this chapter (and then across the state-of-the-art), finding an optimal solution is not an easy task. To overcome this difficulty, it is necessary to develop a design strategy, procedures and algorithms. Hence, one more consideration - technology properties and limits - must be take into account, when a circuit at the transistor-level will meet demanding specifications. Especially, in the cases when submicron and sub-100nm CMOS process is desired (digital on top, digital part of the system must satisfies several specification, etc.)

On account of the previous discussion, these circumstances are arising from the following comments:

- There is no general analog design methodology compared to digital design. Analog design flow is based on iterative process and in most cases the "trail error" loop is performed.
- There is no general design flow of how to deal with the different levels of abstraction, where the transistor-level, circuit-level and system-level complexity of the $\Sigma\Delta$ topic are considered.

On account of the previous discussion and comments, the questions that need answers are:

- How to deal with complexity of the $\Sigma\Delta$M, and the derivation of demanding specifications?
- How to size analog circuits and MOSFET devices to achieves the required performance?

- How to estimated the technology limits?
- How to optimize the system at the different level of abstraction and find the best design trade-offs?
- How to encapsulate expertise and knowledge at different abstraction levels (transistor-level, circuit-level, system-level)?

This section describes proposed approach that prefers simplification of complex problems and global design strategy. The methodology is based on the combination of three aspects (i) analytic description of circuit-level parameters; (ii) numeric look-up table properties of NMOS/PMOS (technology depended data); and (iii) system-level parameters (N-dimensional matrices) of $\Sigma\Delta$M as a product of an analysis, synthesis and simulation.

This methodology is able to identify problems and solutions for a large variety of architectures and their circuit implementation. Also technology limits of the developed system or a block can be recognized at different abstraction levels.

The proposed design strategy is shown in Figure 3.4. Design process starts with three parameters that must be defined (by design architects, customers, an earlier version of the system, etc.). Without these specifications, there is no sense to develop system due to non-optimum solution. In our case (considering Figure 3.4), The first, oversampling frequency, f_{OSR}, is determined by the report rate and a number of channels. The second, the voltage domain is defined by technology libraries and the third, SNR is specified by AFE. Section 3.4 describes a basic analysis of AFE specifications as an example of the complex design strategy that is focused on touchscreen applications.

First of all, noise matrices are computed with ration of Vn_{th}/Vn_{tot} (the initial value of 0.75). If coefficients of the modulator and the voltage domain are defined, the capacitance matrix is computed based on determined values of quantization and thermal noise. Also the swing on modulator nodes must be specified. It should be noted, that these parameters may not be available or may be the subject of an optimization. The synthesis of the modulator is performed for given input parameters (modulator order, a number of quantization levels, a type of the topology, position of NTF zero and OBG) that will achieve the demanding SNR. This design step determines coefficients of the modulator and then the parameters related to system-level and circuit-level can be computed:

- timing specification of an integrator as a function of the report rate of the panel and OSR value. However, it should be considered, that the

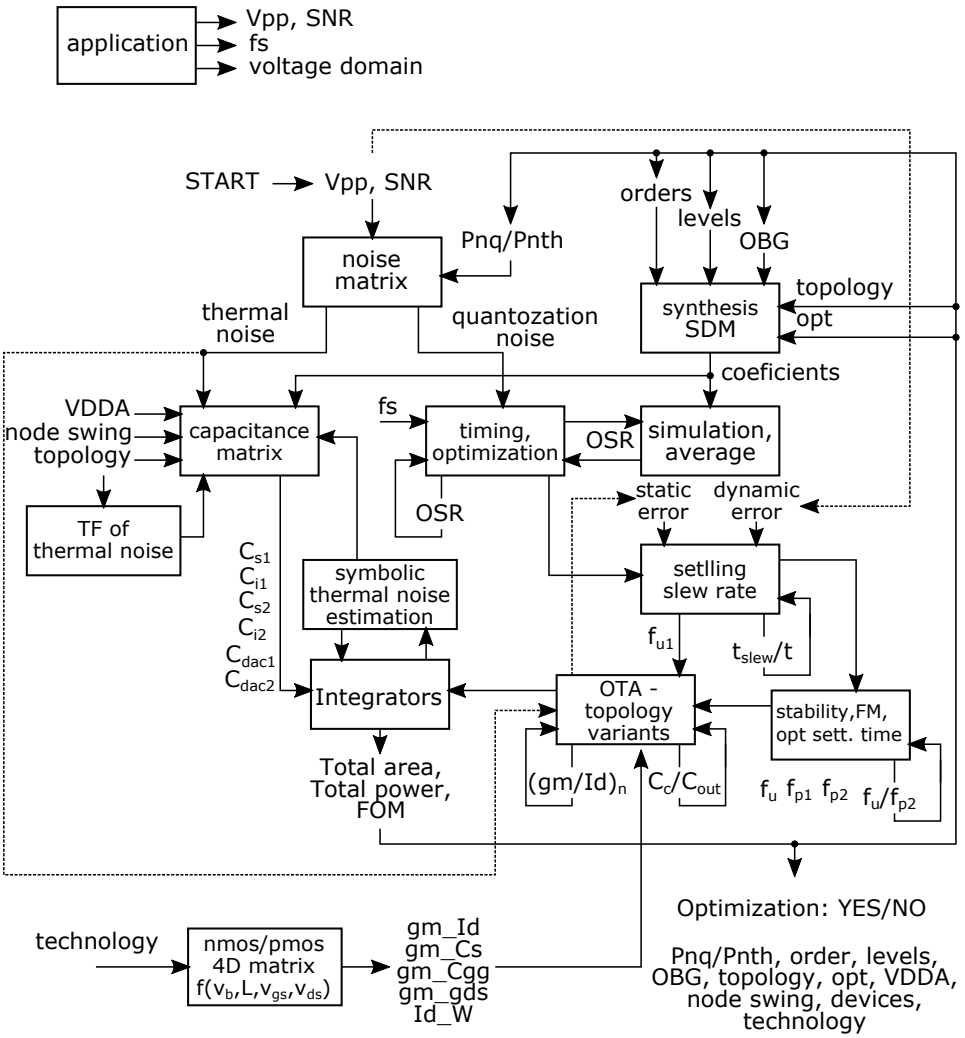

Figure 3.4: Proposed design strategy based on set of python scripts.

value of oversampling ratio is related to amount of quantization noise and can be optimization parameter. These system-level specifications allows to specify following parameters at circuit-level.

- capacitance matrices of the modulator based on the transfer function of thermal sources in the modulator. The value of oversampling ratio and an expression of total thermal noise contribution (from switches and amplifiers) are required in this calculation. The noise contribution

is estimated by a set of symbolic equations that describe noise sources of integrators.

Next chapter is focused on modeling and validation of $\Sigma\Delta$M, which is an important topic of the system validation.

4 | Modeling and Validation of Sigma-Delta Converters

The complexity of electronic systems leads to designing huge and complicated circuits. In most cases, a mixed-signal SoC is desired. The design and verification of these types of circuits must be complex [1] and models of elements at different levels of abstraction are desired.

4.1 Modeling of Sigma-Delta Converters

Figure 4.1 presents steps of the design using levels of abstraction. Also parameters of the abstraction are shown as a design aspect.

- **Behavioral modeling** is focused on an architecture of the ADC or the topology of a ΣΔM. Mathematical representations of the systems are analyzed and the ideal behavior of the system is obtained. Some distortion can be analyzed depending on the parasitic extraction of the second-level effect. Usually, the target technology is not taken into account when the system is verified on the behavioral level.
- **Circuit-level modeling** is focused on the modeling of a circuit-level implementation. Types of cells (like amplifiers, comparators, Digital to Analog Converter (DAC)), are considered and simulated. The parasitic effect such as gain limitation, offset, etc. are investigated based on the target technology. Results of the second-order effect can be incorporated into behavioral models. Then the speed of the verification can be increased.
- **Modeling of a physical implementation** is the final phase of the design. Chosen architecture is built of cells which were implemented

[1] The analog and digital part of the circuit need to be simulate together

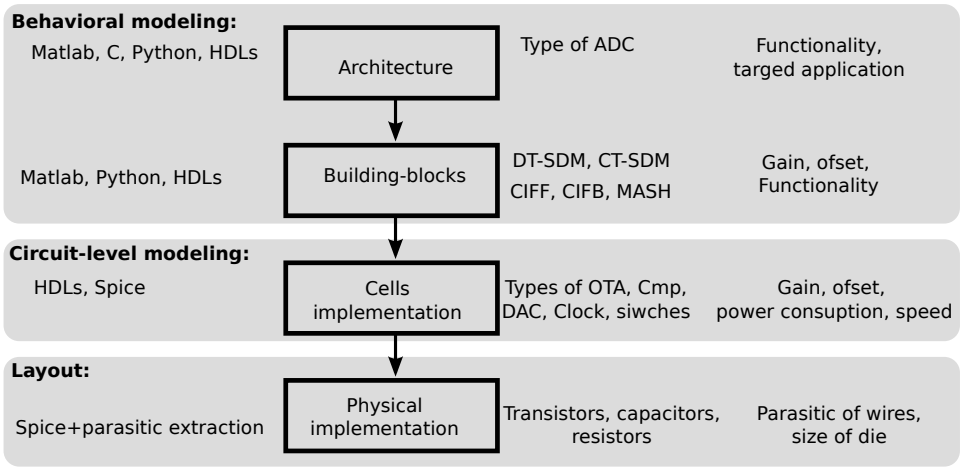

Figure 4.1: Levels of abstraction in the top down design of mixed-signal systems applied to Sigma-Delta ADCs ($\Sigma\Delta$ADC*s)*

.

into the target technology. Parasitics of the wires are extracted and a system is resimulated to ensure that the required performance is achieved.

4.1.1 Configuration of Test Benches

A sin wave with the frequency f_{in}, is applied to the input of a modulator. The sampling frequency, f_s kHz, is an imaginary frequency and is used only as the conversion coefficient to obtain an oversampling frequency, $f_{osr} = f_s OSR$. The output of modulators is bit-stream as is shown in Figure 4.2. We are interested in the frequency spectrum of a modulator, which can be obtained by the Fast Fourier Transform (FFT). There are direct relationship between a number of points, $NBPT$, used by FFT and a resolution of the frequency domain, f_{res}:

$$NBPT = \frac{f_{OSR}}{f_{res}} \tag{4.1}$$

For the particular resolution and rate of an output modulator's bit-stream, the number of points can be defined. For example, to obtain 4096 bits, the transient analysis of 64ms must be performed if the oversampling ratio is set to 64. The resolution in frequency domain, $f_s = \frac{f_s OSR}{NBPT}$, is then 15.625 Hz.

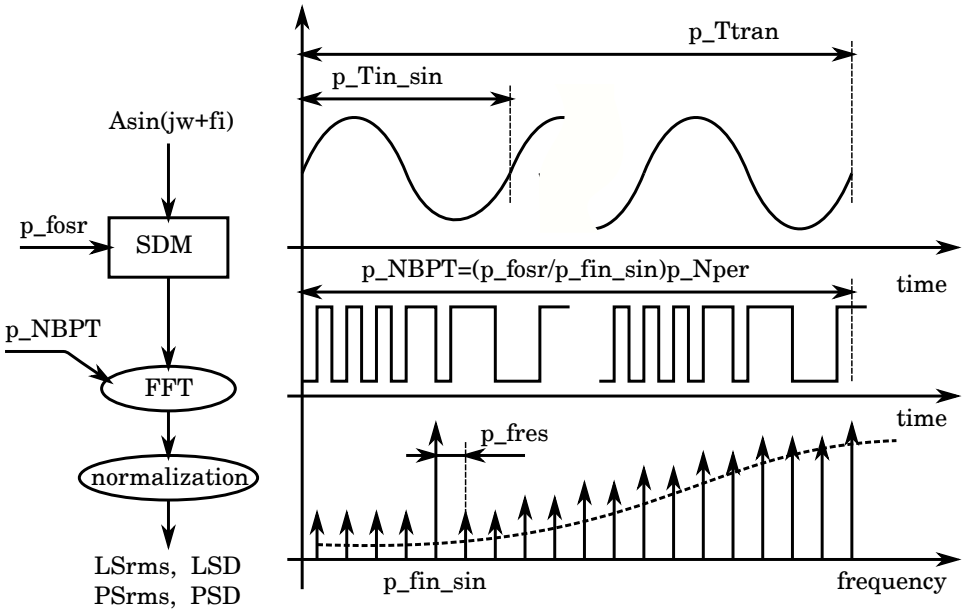

Figure 4.2: Configuration of testbech applied to an evaluation of modulator performance.

Proposed test benches, written by ELDO scripts, are fully parameterized for effective validation of a modulator. It should be noted that for the same resolution, $f_{res} = 15.625Hz$, the time of the transient analysis does not change. N_{per} denotes how many periods of an input sinusoidal signal are needed to reached the particular resolution of the frequency spectrum.

4.1.2 Frequency Spectrum of Modulators

Spectral properties can be obtained by Dicrete Fourier Tranform (DFT), where a vector of N numbers $x_k,\ k = \{0, \ldots, N-1\}$ is transformed into a vector of N complex numbers $y_m,\ m = \{0, \ldots, N-1\}$. To obtain DFT, algorithms called FFT is preferred in many cases. The FFT embedded in ELDO offers two type of normalization: (i) multiplying by $2/NBPT$, default option and (ii) no normalization. In case of the latter, the definition of FFT can be written:

$$Y_m = \sum_{k=0}^{N-1} x_k e^{-2\pi i \frac{mk}{N}}, m = 0, \ldots, N-1, \tag{4.2}$$

The input data of FFT algorithm, x_k, is purely real (reference voltages

of DAC), what result in symmetry $Y_{N-m} = Y_m^*$, where Y_m^* denotes complex conjugation. In the case of testbench, number of points ,$NBPT = 4096$, is even, then Y_0 and $Y_{NBPT/2}$ are real and the upper half of the vector, $\{Y_{NBPT/2+1}, ..., Y_{NBPT-1}\}$, in never computed. The result of FFT is vector, $\{Y_0, ..., Y_{NBPT-1}\}$ of data composed by the real part and the imaginary part:

$$\begin{aligned} Y_m &= \mathrm{Re}(Y_m); \quad m = 0, ..., N/2 \\ Y_m &= \mathrm{Im}(Y_m); \quad m = N/2+1, ..., N-1 \end{aligned} \tag{4.3}$$

Magnitude vector of the output could be rewritten:

$$\vec{Y_{mag}} = \sqrt{\mathrm{Re}(\vec{Y_m})^2 + \mathrm{Im}(\vec{Y_m})^2} \tag{4.4}$$

Basically, the spectral estimation problem can be expressed by the formulation: *"From a finite record of stationary data sequence, estimate how the total power is distributed over frequency"* [Pal16]. There are several different convention to normalized Power Spectrum (PS) which is also called Power Spectral Density (PSD).

Suppose sigma-delta bitstream as the signal (data length is $OSR\ f_s$) then the Fourier transform exists and the PSD can be obtained by two operations (i) autocorrelation + Fourier transform, (ii) Fourier transform + magnitude squared. In that case of (ii) the estimation of PSD is called the periodogram and is defined by the $N/2+1$ frequency bins [SM05], as follows:

$$P(0) = \frac{{Y_{mag}}^2(0)}{NBPT^2},\ P(N/2) = \frac{{Y_{mag}}^2(N/2)}{NBPT^2} \tag{4.5}$$

$$P(f_m) = \frac{{Y_{mag}}^2(f_m) + {Y_{mag}}^2(N-f_m)}{NBPT^2}, \quad f_m = 1, ..., (NBPT/2) - 1, \tag{4.6}$$

4.2 Validation of ΣΔM Sub-blocks

After parameters of circuits are estimated (current consumption, linear settling, slew-rate, frequency characterization and etc.) several tesbenches are created at transistor-level abstraction. This design step is very complex, time consuming, and also licence consuming. The full verification process needed before tapeout can take several months depending on numbers for verification/design engineers.

5 | Transistor-level implementation of the $\Sigma\Delta$M

There are several mosfet models developed across past decades with different accuracy and complexity [Liu01, Bha09, Enz06]. Due to sub-100nm technology, accurate models like PSP or BSIM6 are extremely complex as a consequence of reflecting the real device characteristic. Hand calculations based on the square-law, mostly refereed in many textbook related to analog IC design, give results, which are inaccurate in comparison to the circuit simulations. As a result of the reason that has just been mentioned, majority of designers tend to the procedures based on the iterative and in most cases time-consuming SPICE-based adjustment.

The problem with iterative sizing procedure is that designer loses the deep understanding of the trade-offs in comparison to equations-based design also the ability to identify fundamental issues and limits of the circuit architectures is eluded. This work has been adopted an idea of the device characterization presented in [PGAJ17]. This method enable us to link the device parameters and circuit-level proprieties, which are derived from system-level descriptions.

To adopt this device characterizations, set of Python script has been developed. The main idea of developed procedure is displayed in Figure 5.1, where in the first step, the SPICE simulation of the device is performed. In the second step, device properties are saved to CSV files. Third step illustrates the creation of 4-D matrices, which describe the device properties.

The main differences compared to Murmann approach [PGAJ17] are: (i) no licence of MATLAB is needed, (ii) no specially in-built functions, which enable connection between the look-up engine and the Virtuoso. Then the proposed methodology can be easily used to interact with another SPICE-like simulators.

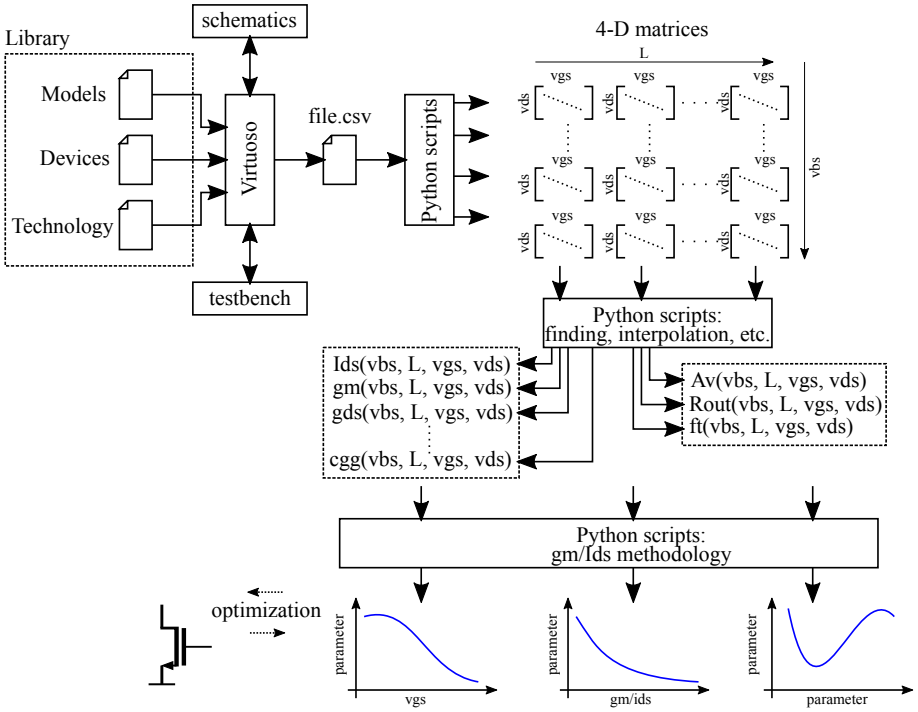

Figure 5.1: Methodology of device characterization by Python scripts.

5.1 Operational Amplifiers

Operational amplifiers, op amps, are an intristic part of many analog and mixed-signal subsystems and systems. Generally, op amps could be defined as high-gain differential amplifiers and are designed to implement in a feed-back systems. The open-loop gain is typically in the range of 10^2 to 10^5 depending on topology and technology.

The operational amplifier as the essential component of switched-capacitor circuits needs special attention during the designing phase. Demand for low-power implementation of circuits, general-purpose Operational Amplifiers (op-amps) can not satisfy the power-consumption requirements of modern systems.

This summary of OTA topologies given by [Raz01] serves only rough estimation and moreover, the variation of these parameters are related to technology and the size of devices. For example, the variation of open-loop gain is presented by the next experiments.

The Figure 5.4 shows open-loop gain of the simple single-stage OTA,

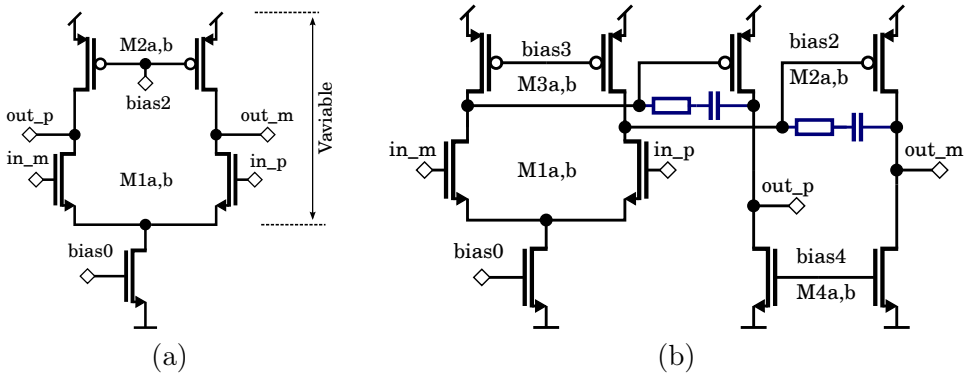

Figure 5.2: Differential OTAs: simple single-stage OTA with the best FOM (a), two-stage OTA with the Miller compensation (b).

5.2 (a), as a function of two parameters: length of the pmos device (active load), L_p, and length of the nmos device (differential pair), L_n. The Folded cascode, the schematic is displayed on Figure 5.3(b), offers bigger DC voltage gain as a consequence of an increasing value of the output resistance. The Two-stage amplifier, 5.2 (b), is another option of the increasing DC voltage gain, $A_{V,2STAGE} = gm_1 R_{out1} gm_2 R_{out2}$.

The evaluation has been provided for two technology nodes, 65nm and 180nn. Variations of low-frequency gain (related to different technologies) are illustrated by the comparing results of Figures 5.4 and 5.5 corresponding to simple one-stage OTA. The summary of OTA topologies is listed in Tables 5.1 and 5.2. Results are specified for values of length, $L_p = L_n = 400\,nm$, values of transconductance efficiency, $(gm/Ids)_{Mx} = 15\,S/A$. The analysis has been provided for other two OTA topologies, but results are not presented in the report.

Owing to the fact that current consumption is directly linked to the GBW, noise performance, low frequency open-loop gain, operation amplifier must be design for specific application with determined parameters.

Considering the application, the OTA metrics can be established as a consequence of the input parameters and the optimization parameters.

- *voltage gain:* determined by the allowable distortion of the $\Sigma\Delta$ loop. Exact value can be obtain by the time-domain simulation,

- *frequency bandwidth*: determined by the report rate of the system, the number of channels, slew rate and dynamic error ($\sim$ linear settling time),

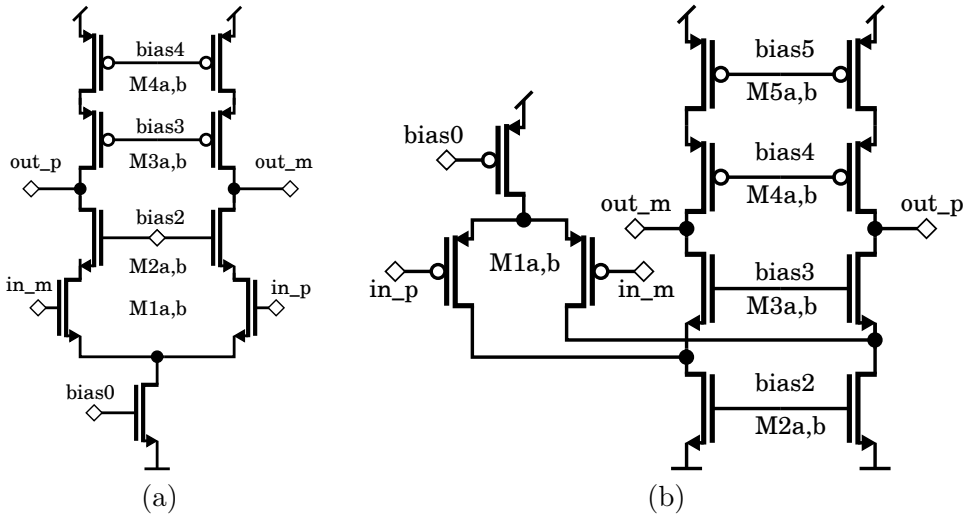

Figure 5.3: Techniques used to increase gain of a op amp: the telescopic cascode (a), the folded cascode (b).

- *systematic and random offset:* determined by the system requirements. The exact value can be obtain by the corner simulation (Process-Voltage-Temperature),

- *total output integrated noise:* defined by the topology of ΣΔM, OSR, the ratio of total thermal noise and total noise. Special attention should be paid to the decomposition of the total sampled noise of the first stage (first integrator). Total sampled thermal noise at the integrator output is the sum of the first and the second clock phase: $v_{ntot}^{intg} = v_{n,ph1}^{SW} + v_{n,ph2}^{SW} + v_{n,ph2}^{OTA}$,

- *input/output voltage range:* determined by the input/output common-mode voltage, voltage domain, saturation of the MOSFET devices and topology of the OTA,

- *slew rate:* is not an input parameter. Slew rate is a result, which is determined by the total load capacitance, C_{Ltot}, seen at the output (or the compensation capacitance, C_c, in the case of two-stage OTA) and the current of the differential pair, I_{TAIL}.

- *power consumption:* is not an input parameter. Power consumption is a result (product) of parameters discussed above.

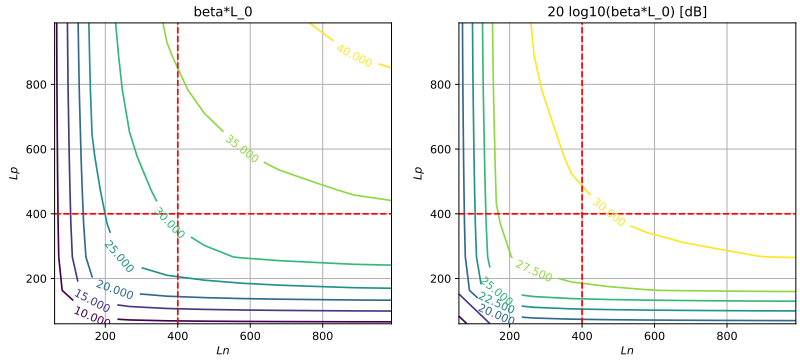

Figure 5.4: Low-frequency loop-gain for simple differential OTA. Feedback factor, β, is near to one. Estimation has been performed for 65 nm technology and 1.2V devices.

Topology	Gain	Output swing [V]	Speed	Power Diss.	Noise
Simple	29.5	0.6	$\propto 1/ts, \epsilon_d$	High	$\propto C_{Ltot}$
Folded Cascode	38	0.4	$\propto 1/ts, \epsilon_d$	Medium	$\propto C_{Ltot}$
Two-stage	59	0.8	$\propto 1/ts, \epsilon_d$	Medium	$\propto C_{Ltot}, C_C$

Table 5.1: Ota metrics for the Simple one-stage OTA, 5.2 (a), Folded Cascode OTA 5.3 (b), and Two-stage OTA with the miller compensation. The estimation has been provided by the python script, that uses real data of the MOSFETs (1.2 device, technology node is $\approx 65\,nm$). The parameter of devices are follows: $(gm/Ids)_{Mx} = 15$, $L_n = L_p = 400\,nm$, VDD = 1.2V.

5.2 Regenerative Latch-based Comparators

Regenerative latch-based and pure dynamic comparators use clock signal to define time of the compare operation. In others words, comparator works in the discrete-time.

The general concept of this type comparator is shown in Figure 5.6. The first stage could be the same as the family of continuous-time comparators. The second, regenerative latch, forces the latch nodes to full-scale range during the tracking phase. There are many concepts of the possible latch depending on the (equilibrating) reseting operations. The last stage, Set-Reset latch, is used to save the value of the comparator's outputs.

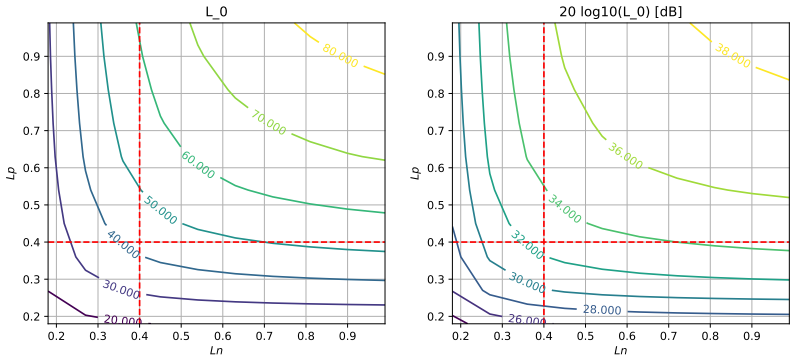

Figure 5.5: Low-frequency loop-gain for simple One-stage OTA. Feedback factor, β, is near to one. Estimation has been performed for 180 nm technology and 1.8V devices.

Topology	Gain	Output swing [V]	Speed	Power Diss.	Noise
Simple	32.5	1.2	$\propto 1/ts, \epsilon_d$	High	$\propto C_{Ltot}$
Folded Cascode	49	1	$\propto 1/ts, \epsilon_d$	Medium	$\propto C_{Ltot}$
Two-stage	69	1.4	$\propto 1/ts, \epsilon_d$	Medium	$\propto C_{Ltot}, C_C$

Table 5.2: Ota metrics for the Simple one-stage OTA, 5.2 (a), Folded Cascode OTA 5.3 (b), and Two-stage OTA with the miller compensation. The estimation has been provided by the python script, that uses real data of the MOSFETs (1.8 device, technology node is $\approx 180\,nm$). The parameter of devices are follows: $(gm/Ids)_{Mx} = 15$, $L_n = L_p = 400\,nm$, $VDD = 1.8V$.

The elimination of static components of current lead to pure dynamic comparators. Considering figure 5.6, the preamplifier can be taken out to improve consumption of the circuit. It should be noted, there is no best topology of the dynamic comparator; application, target technology, voltage headroom, input swing and speed must be taken to account when the comparator is designed.

5.2.1 One-stage Dynamic Comparators

Basic one-stage dynamic comparators are shown in Figure 5.7 [Sch05]. The outputs, Lo_m, Lo_p are internal nodes of the comparator and are reset by

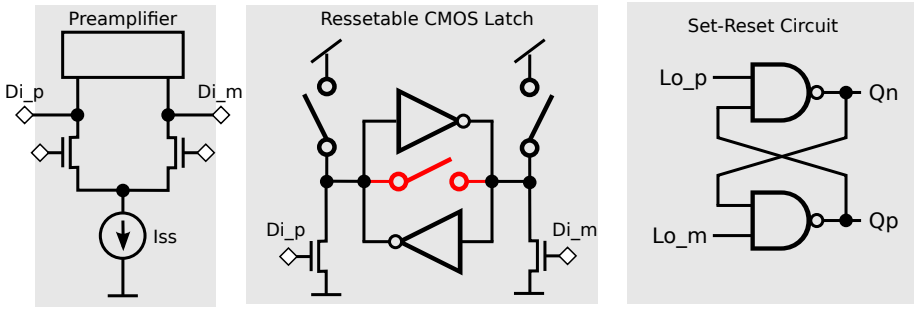

Figure 5.6: The concept of regenerative latched-based comparators.

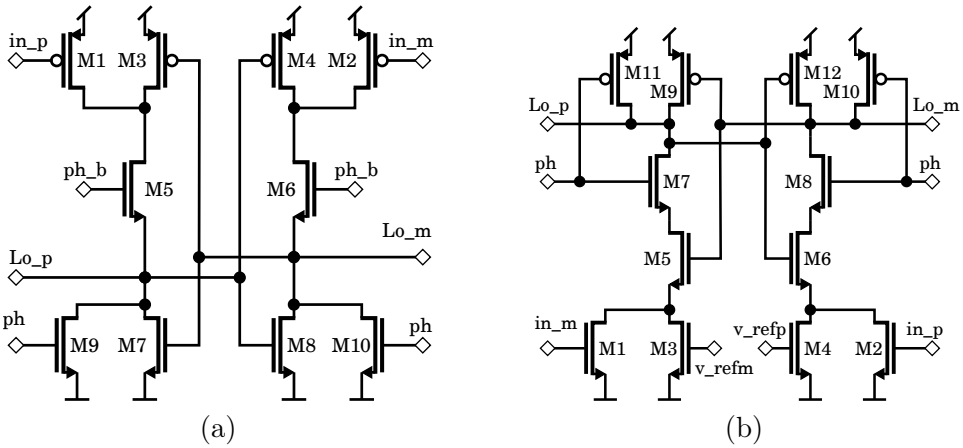

Figure 5.7: Types of dynamic comparators: the basic one-stage comparator (a), Lewis-Gray comparator (b).

every clock event. Then a result must be stored. In general, the RS-latch can by used for this purpose. These two comparators are redesigned to the technology $\approx TSMC130$. The positive supply rail, VDDA, is equal 1.2V and the negative supply rail, VSSA, is equal to 0V.

The second topology, called Lewis-Gray Comparator, is showed in figure 5.7 (b) [HZCG08] and [HZCG09]. The circuit uses four transistors in the stack, then this circuit is not suitable for low-voltage implementations. In the reset phase, $ph = 0$, the outputs are precharged to VDDA rail. The NMOS switches (M7, M8) are off; then no DC current flows via the stacks.

Sophisticated types of one-stage dynamic comparators are shown in Figure 5.8. The topology showebd in Figure 5.8 (a) [Sch05] are derived from the basic latched comparator [Riv15] and improves shortcoming of previous

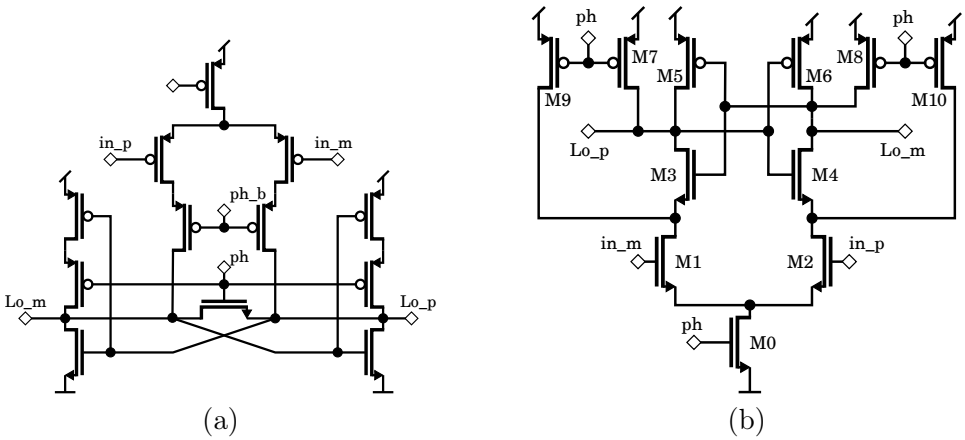

Figure 5.8: Types of dynamic comparators. One-stage comparator (a), strongArm comparator (b).

topologies, but overlap capacitance is still a problem. A very popular topology, called StrongArm [NBTdP08], is shown in figure 5.8 (b). As previous topologies, the circuit is driven using two clock phases:

- *the reset phase*, $ph = 0$, resets the stored value and prepares a comparator to the new evaluation process.
- *in the evaluation phase*, $ph = 1$, capacitance of internal nodes are discharged and the cross-coupled inverters restore digital levels.

5.2.2 Two-stage Dynamic Comparators

One-stage comparators are discussed in 5.2.1. The main problem of these topologies is the tradeoff between the speed and resolution/offset. Both are affected by the tail current. The problem is solved by sealing the supply currents of the first and second stage. The first stage, a dynamic preamplifier, integrate the difference voltage during the sampling, propagation time. To increasing the resolution of the fist stage the tail current of the preamplifier is decreasing. The second stage, the dynamic latch, is primary used for the restoration of the amplified input voltage. To increasing the speed of the comparator the currents of the latch are increased.

6 | Conclusions

In this doctoral thesis, several aspects associated with a role of the sigma-delta modulation in a touchscreen system have been introduced. This section summarizes the main contributions of this work and proposes directions for future work. Author's publication are listed at the end of the thesis.

6.1 Summary

This work deals with the wide scope of the state-of-the-art, which including sensors, analog and mixed-signal systems, integrated circuit design and low-power optimization. Therefore, the summary of the work presented by this thesis will be divided to three parts.

The first part is dedicated to **the system application**. A touchscreen system based on projective-capacitance has been studied and a basic model of a sensor has been created. A survey of ADCs focused on low-power and area-efficient implementations has been provided. Results of the survey identify a possible, low-power, area-efficient solution based on ΣΔMs.

The second part deals with **system-level focused on the sigma-delta modulation**. First, the state-of-the-art of ΣΔM has been introduced, where the large variety of modulators has been presented. Therefore, two ΣΔMs implementations - examples of DT-ΣΔM and CT-ΣΔM, which need different design strategies - with a particular test bench and a timing circuit were proposed and validated. Although these modulators allow deep study and observation of the effects (caused by non-ideal circuits), no best low-power solution can be identified. This statement is proven by the wide scope of the state-of-the-art, focused on sigma delta converters.

The wide scope of the research carried out on sigma-delta modulation makes the design steps and decisions more and more complicated. On the side of circuit-level we face problems of decisions related to the right architecture. On the other side, system-level, we do not take into account circuit

limits. Hence, technology properties and limits must be take into account, when the circuit at the transistor-level should meet the demanding specification. The large variety of modulators and the wide diversity of circuit implementations result in complex scenario where design strategy is not evident at sight. The third part **provides an structural methodology as the solution to these concerns**.

We can conclude, that every application has a unique optimal solution, which comes from the parameters of the developed system. As a result of the reasons that have been mentioned, the main question "How to identify best architecture and implementation of ΣΔM?" arises with even more importance than the question "Which type of the modulator architecture we should choose to achieve best power-consumption or silicon-area trade-offs?".

To answer this question, we first performed analysis and exploration of several aspects at the different abstraction levels. And then, systematic design strategy, procedures and algorithms have been developed to provide:

- an identification of circuit metrics from the system-level abstraction,
- an identification limits of technology process,
- the topology selection at transistor-level,
- an optimization circuit-level metrics such as bias currents, capacitance values, sampling frequency, input/output voltage swing,
- an identification of fundamental circuit limits,
- the circuit sizing procedure (suitable values for particular devices such as Ids, W, L).

These functions have been integrated together and with combination of the proposed design strategy and procedures, the first version of the design assistance tool has been created. This design assistance tool can be applicable:

- to provide the first level prototyping of the new system based on the sigma-delta modulation,
- to provide an estimation of Design Migration and IP Porting of the system,
- to provide a leading-edge innovation as a consequence of the solving fundamental issues with a topology of ΣΔM or circuit architecture.

6.2 Future Work

Future research should focus on the extension of design methodologies to continuous-time modulators. This aspect is necessary to validate the power-efficient architecture of the touchscreen systems, that can be drawn from this study and research.

List of My Own Publications

Publication included in this thesis

The publishing activity of the author which corresponds with the content of this thesis:

- **L. Palocko**, "Modeling and validation of ΣΔ modulators," *In 8th International Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT 2016)* pages 310-313, 2016.

  Author's Contribution: The article is focused on modeling and validation of ΣΔM. The levels of abstraction - including behavioral, circuit-level and physical modeling of analog integrated circuits - are discussed. A behavioral modeling is presented and macromodels of ΣΔM cells are introduced. In addition, different architectures of a ΣΔM are validated with the discussion of a ΣΔM spectrum and normalization of Fast Fourier Transform (FFT) results.

- **L. Palocko**, "Spectrum of the sigma delta modulation," *In Electronics and Informatics 2016., Pilsen: University of West Bohemia* pages 129-132, 2016.

  Author's Contribution: – The objective of this paper is describe spectrum of the sigma delta modulation and their normalization to the Power Spectral Density (PSD). The drawbacks of the normalization are discussed and the simulation of the sigma delta bitstream is presented.

- **L. Palocko**, "An Offset Analysis of One-stage Dynamic Comparators," *In Electronics and Informatics 2015., Pilsen: University of West Bohemia* pages 183-186, 2015.

  Author's Contribution: The author investigated an offset of popular topologies of One-stage dynamic comparators. The simulations were based on the Generic Design Kit produced by Mentor Graphic.

Publication not included in this thesis

The publishing activity of the author is outside the scope of this thesis:

- TOTEM Collaboration, Diamond detectors for the TOTEM timing upgrade, *Journal of Instrumentation*, pages 0-23, 2017

- TOTEM Collaboration, Evidence for non-exponential elastic proton-proton differential cross-section at low $|t|$ and $\sqrt{s} = 8TeV$ by TOTEM, *Published in : Nucl. Phys. B 899 (2015) 527-546, Geneve*, pages 1-21, 2016

- TOTEM Collaboration, Measurement of elastic pp scattering at $\sqrt{s} =$ 8TeV in the Coulomb–nuclear interference region: determination of the ρ-parameter and the total cross-section, *European Physical Journal C, 2016, Geneve*, 18 page, 2015

- **L. Palocko,**,"Vysokoúrovňové modelovanie jednoduchých zreťazených liniek pre špecifické inštrukčné sady.". In *Electronics and Informatics 2012. Part 2 Electronics.* Pilsen: University of West Bohemia, pages 73-76, 2012.

- J. Moldaschl, **L. Palocko**, and J. Broulim, "Boost power factor topology with average current control," *In 2014 International Conference on Applied Electronics, University of West Bohemia,* 2014.

- **L. Palocko,** "Návrh registrového poľa architektúry ARMv1 a ARMv2.". In *Electronics and Informatics 2013. Part 2 Electronics.* Pilsen: University of West Bohemia, 2013.

- J. Broulim, V. Georgiev, J. Moldaschl, **L. Palocko**, "Ldpc code optimization based on tanner graph mutations," *In 21st Telecommunications Forum (TELFOR) Proceedings of Papers. Belgrade,* pages 389-392, 2013.

- **L. Palocko**, J. Moldaschl, and J. Broulim, "Decoder with the dynamic cmos matrix," *In 21st Telecommunications Forum TELFOR 2013. Belgrade. IEEE*, pages 612-615, 2013.

Bibliography

[Bha09] A. B. Bhattacharyya. *Compact MOSFET models for VLSI design.* John Wiley & Sons (Asia) IEEE Press, Singapore Hoboken, NJ Piscataway, NJ, 2009.

[Enz06] Christian Enz. *Charge-based MOS transistor modeling : the EKV model for low-power and RF IC design.* John Wiley, Chichester, England Hoboken, NJ, 2006.

[HZCG08] Jun He, Sanyi Zhan, Degang Chen, and R. Geiger. A simple and accurate method to predict offset voltage in dynamic comparators. In *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, pages 1934–1937, May 2008.

[HZCG09] J. He, S. Zhan, D. Chen, and R. L. Geiger. Analyses of static and dynamic random offset voltages in dynamic comparators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(5):911–919, May 2009.

[Jon10] B. E. Jonsson. On cmos scaling and a/d-converter performance. In *NORCHIP, 2010*, pages 1–4, Nov 2010.

[Jon11a] B. E. Jonsson. Area efficiency of adc architectures. In *Circuit Theory and Design (ECCTD), 2011 20th European Conference on*, pages 560–563, Aug 2011.

[Jon11b] B. E. Jonsson. An empirical approach to finding energy efficient adc architectures. In *NORCHIP, 2010*, pages 1–6, June 2011.

[Jon13] Bengt E. Jonsson. A/D-converter performance evolution. Technical report, University of Zurich, Department of Informatics, 07 2013.

[Liu01] William Liu. *Mosfet models for spice simulation, including BSIM3v3 and BSIM4.* Wiley-Interscience Publication, New York, 2001.

[Mur] Boris Murmann. Adc performance survey 1997-2015 [online], aviable:. `http://web.stanford.edu/~murmann/adcsurvey.html`.

[NBTdP08] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas. Noise analysis of regenerative comparators for reconfigurable adc architectures. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(6):1441–1454, July 2008.

[Pal16] L Palocko. Spectrum of the sigma delta modulation. *Elektrotechnika a informatika 2016. Elektrotechnika, elektronika, elektroenergetika. Plzeň: Západočeská univerzita v Plzni*, pages 129–132, 2016.

[PGAJ17] Boris Murmann Paul G. A. Jasper. *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables.* Cambridge University Press, Kindle Edition., United Kingdom, 2017.

[Raz01] Behzad Razavi. *Design of Analog CMOS Integrated Circuits.* McGraw-Hill, New York, 2001.

[Riv15] Angelo Rivetti. *CMOS: Front-End Electronics for Radiation Sensors (Devices, Circuits, and Systems.* CRC Press, 2015.

[Sch05] Richard Schreier. *Understanding Delta-Sigma Data Converters.* Wiley-IEEE Press, 2005.

[SM05] Petre Stoica and Randolph L Moses. *Spectral Analysis of Signals.* Upper Saddle River, N.J.: Pearson/Prentice Hal, 2005.

[SP17] Gabor C. Temes Shanthi Pavan, Richard Schreier. *Understanding Delta-Sigma Data Converters, 2nd Edition.* Wiley-IEEE Press, 2017.

[SSST05] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes. Design-oriented estimation of thermal noise in switched-capacitor circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(11):2358–2368, Nov 2005.

[Wal12] G Walker. A review of technologies for sensing contact location on the surface of a display. *Journal of the SID*, 2012.